

EXHIBIT A



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[54] QUADRATURE AMPLITUDE MODULATED DATA FOR STANDARD BANDWIDTH TELEVISION CHANNEL

[75] Inventors: Zheng Huang, Willow Grove, Pa.; Chris Heegard, Ithaca, N.Y.

[73] Assignee: GI Corporation, Hatboro, Pa.

[21] Appl. No.: 184,499

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[51] Int. Cl.⁶ H04L 5/12; H04L 27/36; G06F 11/10; H04N 7/12

[52] U.S. Cl. 375/265; 375/264; 375/261; 375/298; 371/43; 348/384

[58] Field of Search 375/265, 264, 375/262, 261, 298, 341; 371/43; 348/384, 155

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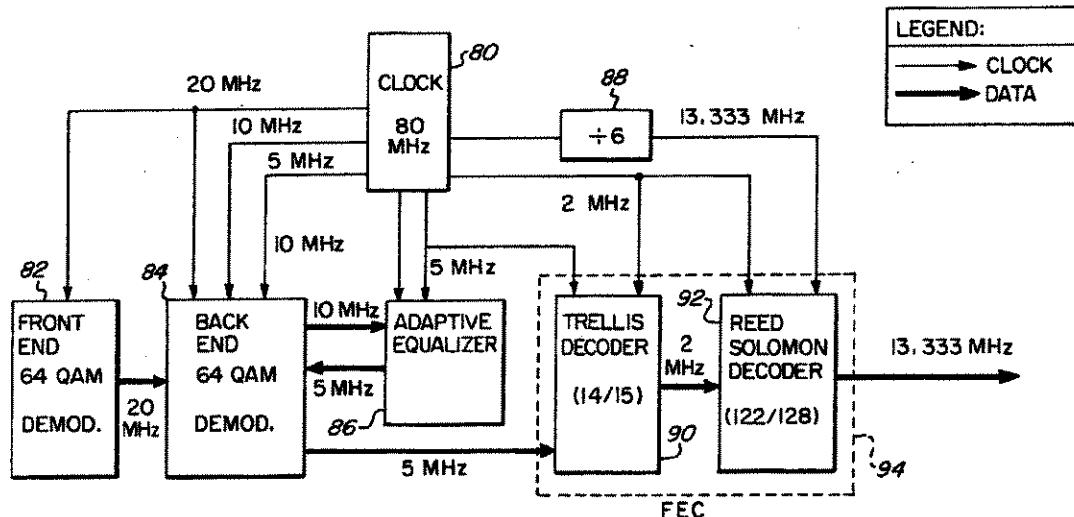
Primary Examiner—Edward L. Coles, Sr.

Assistant Examiner—Allan A. Esposo
Attorney, Agent, or Firm—Barry R. Lipsitz

[57] ABSTRACT

An outer symbol error correcting code is concatenated with a punctured multidimensional trellis code to provide an optimal scheme for communicating digital television signals in a standard (e.g., approximately six MHz) bandwidth channel via a cable television network or the like. An input signal is encoded using an outer symbol error correcting code to produce successive blocks. Each block comprises N seven-bit coded symbols of which M represent information to be communicated and the remaining N-M coded symbols comprise error correcting information. M/N is either 120/126, 121/127 or 122/128. The blocks are interleaved, and may be supplemented with control symbols that include a synchronization pattern for M/N=121/127 or M/N=122/128. The interleaved blocks are convolutionally encoded using an inner trellis code having a punctured rate 4/5 (sixty-four QAM) or 3/4 (sixteen QAM). The output symbols are multilevel modulated for transmission over a communication path using, for example, sixteen or sixty-four QAM. The transmitted symbols are decoded using a trellis decoder, deinterleaved, and further decoded in an outer symbol error decoder concatenated with the inner trellis decoder.

25 Claims, 3 Drawing Sheets



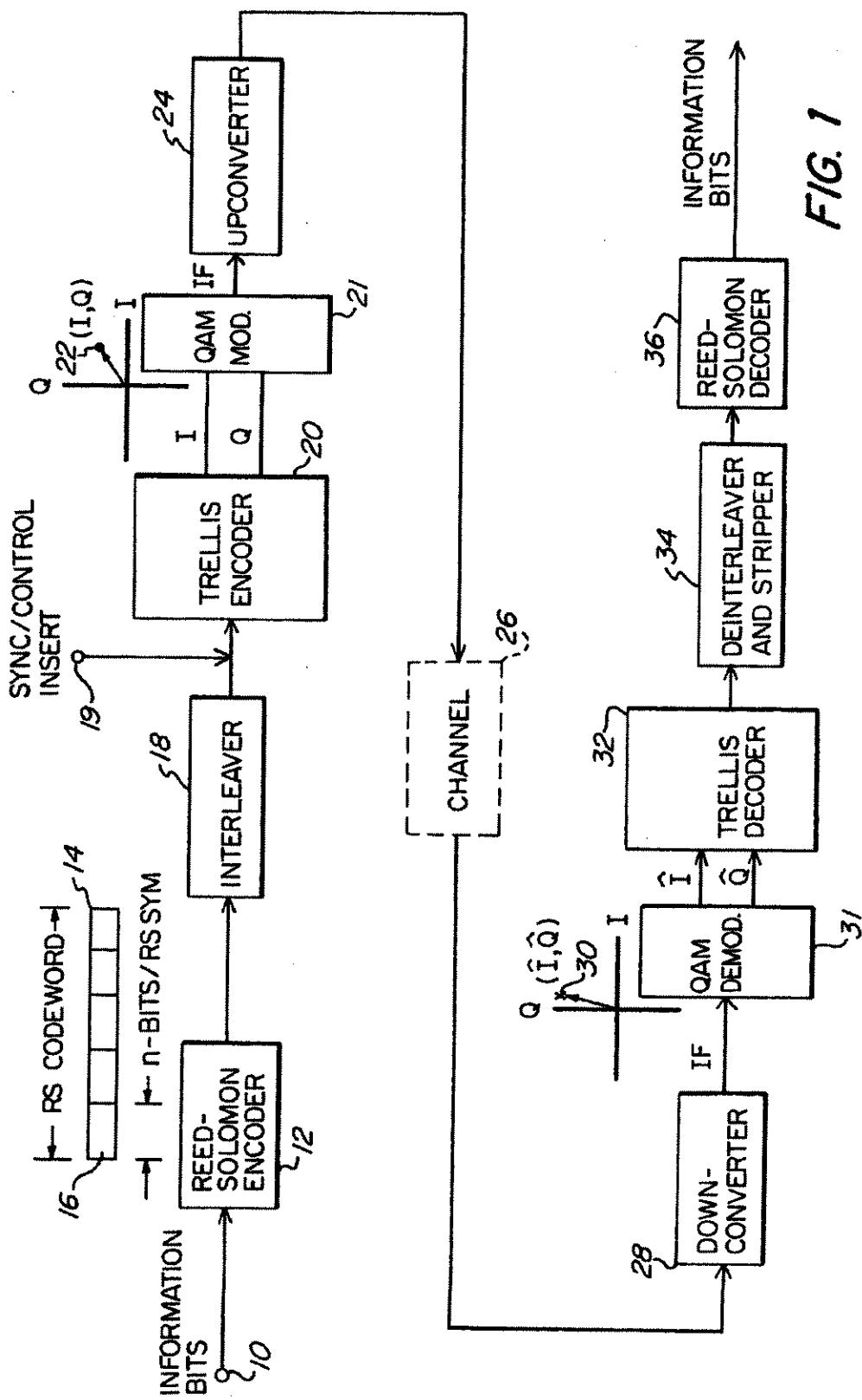
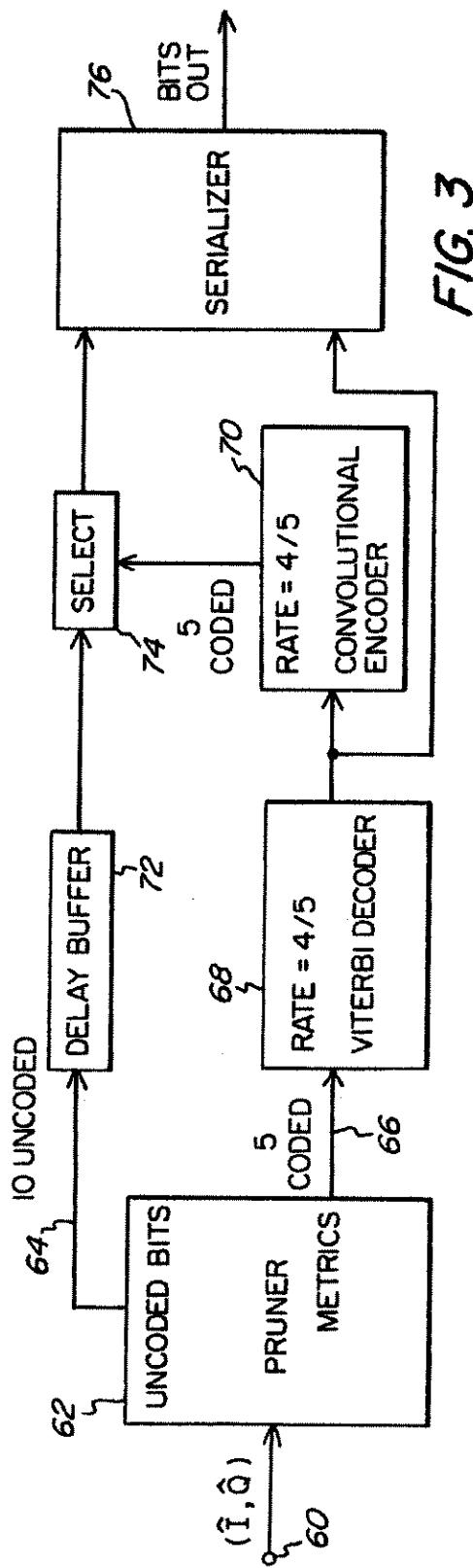
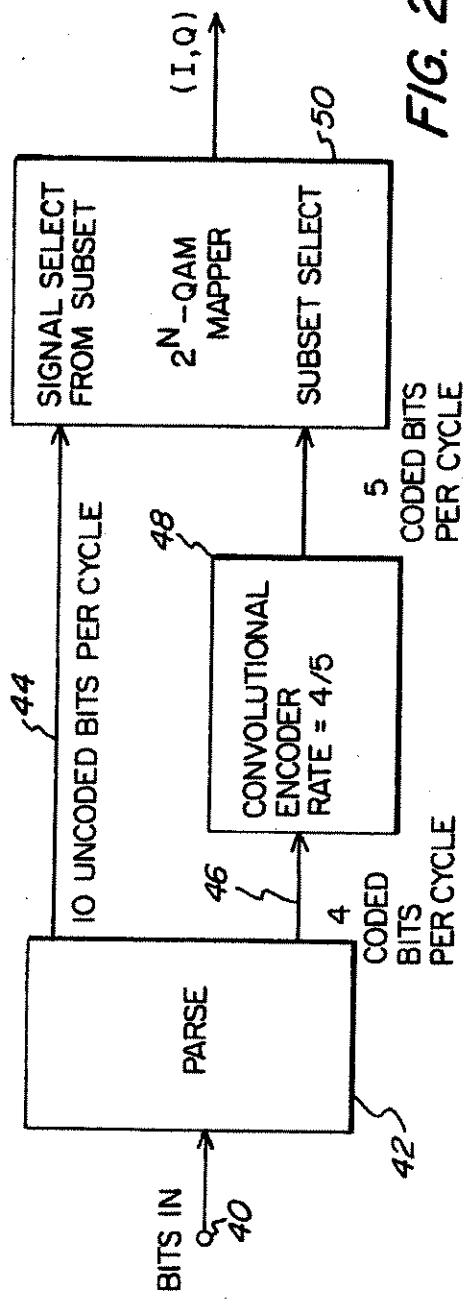


FIG. 1



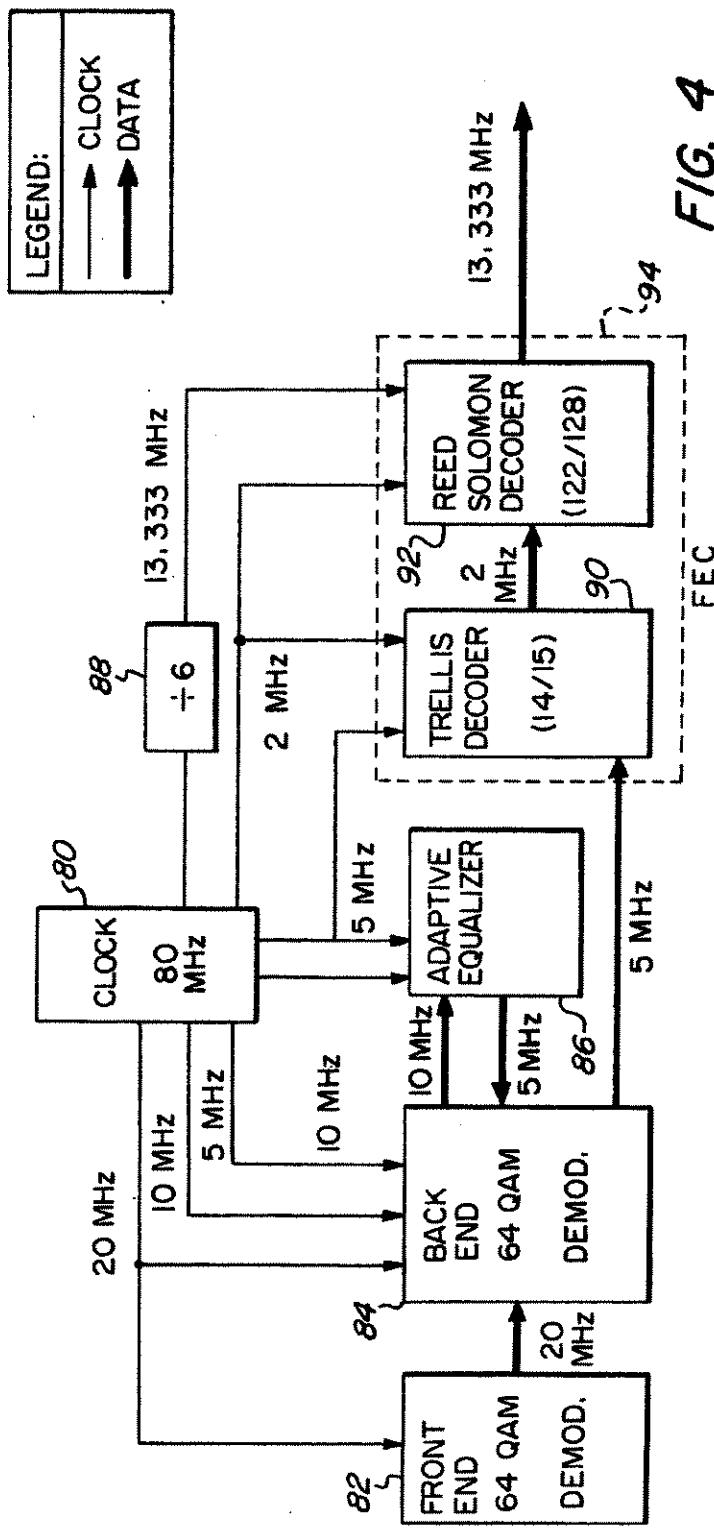


FIG. 4

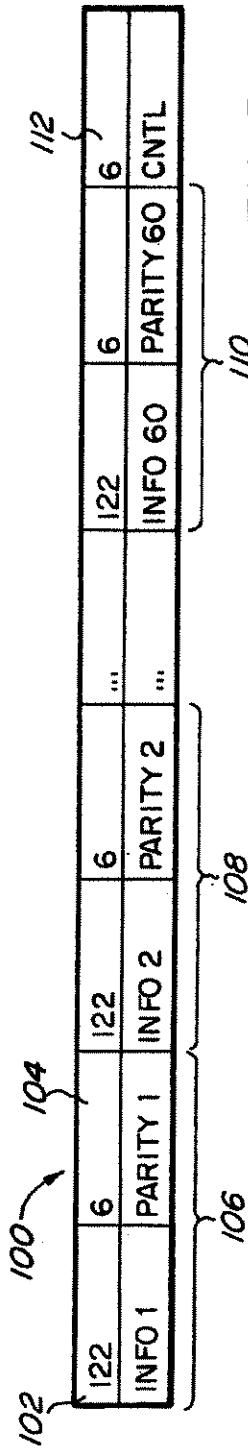


FIG. 5

**QUADRATURE AMPLITUDE MODULATED
DATA FOR STANDARD BANDWIDTH
TELEVISION CHANNEL**

BACKGROUND OF THE INVENTION

The present invention relates to trellis coded quadrature amplitude modulation (QAM) and more particularly to a practical method for coding 16 and 64 QAM transmission to enable a low-cost implementation of a digital cable television system or the like.

Digital data, for example digitized video for use in broadcasting digitized conventional or high definition television (HDTV) signals, can be transmitted over satellite, terrestrial or cable VHF or UHF analog channels for communication to end users. Analog channels deliver corrupted and transformed versions of their input waveforms. Corruption of the waveform, usually statistical, may be additive and/or multiplicative, because of possible background thermal noise, impulse noise, and fades. Transformations performed by the channel are frequency translation, nonlinear or harmonic distortion and time dispersion.

In order to communicate digital data via an analog channel, the data is modulated using, for example, a form of pulse amplitude modulation (PAM). Typically, quadrature amplitude modulation (QAM) is used to increase the amount of data that can be transmitted within an available channel bandwidth. QAM is a form of PAM in which a plurality of bits of information are transmitted together in a pattern referred to as a "constellation" that can contain, for example, sixteen, thirty-two or sixty-four points. An example of a system for communicating digital data using QAM, and specifically trellis coded QAM, is provided in U.S. Pat. No. 5,233,629 to Paik, et al., incorporated herein by reference.

In pulse amplitude modulation, each signal is a pulse whose amplitude level is determined by a transmitted symbol. In 16-bit QAM, symbol amplitudes of -3, -1, 1 and 3 in each quadrature channel (I and Q) are typically used. Bandwidth efficiency in digital communication systems is defined as the number of transmitted bits per second per unit of bandwidth, i.e., the ratio of the data rate to the bandwidth. Modulation systems with high bandwidth efficiency are employed in applications that have high data rates and small bandwidth occupancy requirements. One such application is the transmission of television signals in a standard 6 MHz or so bandwidth. QAM provides bandwidth efficient modulation that is useful for such applications.

Trellis coded modulation (TCM) has evolved as a combined coding and modulation technique for digital transmission over band limited channels. It allows the achievement of significant coding gains over conventional uncoded multilevel modulation, such as QAM, without compromising bandwidth efficiency. TCM schemes utilize redundant non-binary modulation in combination with a finite-state encoder which governs the selection of modulation signals to generate coded signal sequences. In the receiver, the noisy signals are decoded by a soft-decision maximum likelihood sequence decoder. Such schemes can improve the robustness of digital transmission against additive noise by 3-6 dB or more, compared to conventional uncoded modulation. These gains are obtained without significant bandwidth expansion or reduction of the effective information rate as required by other known error correction schemes. The term "trellis" is used because these schemes can be described by a state-transition (trellis) diagram similar to the trellis diagrams of binary convolutional codes. The difference is that TCM

extends the principles of convolutional coding to nonbinary modulation with signal sets of arbitrary size.

For applications that are band limited, and require low cost components (particularly low cost data decoders), conventional QAM systems have not been feasible due to the complexity and relatively high cost of the required encoder and decoder circuits. In fact, it is typical to implement QAM trellis encoders and decoders in expensive custom integrated circuit chips.

One band limited application in which a low cost solution is necessary for communicating digital data is the digital communication of cable television signals, which may include compressed conventional or high definition television signals. Systems for transmitting such signals have data rate requirements on the order of 15-30 megabits per second (Mbps), bandwidth occupancy requirements on the order of 6 MHz (the bandwidth of a conventional National Television System Committee (NTSC) television channel), and very high data reliability requirements (i.e., a very small bit error rate). The data rate requirement arises from the need to provide a high quality compressed television picture. The bandwidth constraint is a consequence of the U.S. Federal Communications Commission requirement that such signals occupy existing 6 MHz television channels, and must coexist with the current broadcast NTSC signals. Similar constraints are mandated by the PAL (Phase Alternating Line) and SECAM (Sequential Color and Memory) television systems used outside the U.S.

The combination of data rate and bandwidth occupancy requirements mandated by the standard television transmission systems dictates a modulation system that has high bandwidth efficiency. Indeed, the ratio of data rate to bandwidth must be on the order of 3 to 6. This means that a bandwidth efficient modulation such as QAM is required. However, as noted above, QAM systems have been too expensive to implement for high volume consumer applications.

The requirement for a very high data reliability in digitized video applications results from the fact that highly compressed source material (i.e., the compressed video) is intolerant of channel errors. The natural redundancy of the signal has been removed in order to obtain a concise description of the intrinsic value of the data. For example, for a system to transmit at 15 Mbps for a twenty-four hour period, with less than one bit error, requires the bit error rate (BER) of the system to be less than one error in 10^{12} transmitted bits.

Data reliability requirements are often met in practice via the use of concatenated coding techniques, which is a divide and concur approach to problem solving. In such a coding framework, two codes are employed. An "inner" modulation code cleans up the channel and delivers a modest symbol error rate to an "outer" decoder. The inner code is usually a coded modulation that can be effectively decoded using "soft decisions" (i.e., finely quantized channel data). A known approach is to use a convolutional or trellis code as the inner code with some form of the "Viterbi algorithm" as a trellis decoder. The outer code is most often a t-error-correcting, "Reed-Solomon" code. Such Reed-Solomon coding systems, that operate in the data rate range required for communicating digital television data, are widely available and have been implemented in the integrated circuits of several vendors. The outer decoder removes the vast majority of symbol errors that have eluded the inner decoder in such a way that the final output error rate is extremely small.

A more detailed explanation of concatenated coding schemes can be found in G. C. Clark, Jr. and J. B. Cain,

"Error-Correction Coding for Digital Communications", Plenum Press, New York, 1981; and S. Lin and D. J. Costello, Jr., "Error Control Coding: Fundamentals and Applications", Prentice-Hall, Englewood Cliffs, N.J., 1983. Trellis coding is discussed extensively in G. Ungerboeck, "Channel Coding with Multilevel/Phase Signals", *IEEE Transactions on Information Theory*, Vol. IT-28, No. 1, pp. 55-67, January 1982; G. Ungerboeck, "Trellis-Coded Modulation with Redundant Signal Sets—Part I: Introduction,—Part II: State of the Art", *IEEE Communications Magazine*, Vol. 25, No. 2, pp. 5-21, February 1987; and A. R. Calderbank and N. J. A. Sloane, "New Trellis Codes Based on Lattices and Cosets", *IEEE Transactions on Information Theory*, Vol. IT-33, No. 2, pp. 177-195, March 1987. The Viterbi algorithm is explained in G. D. Forney, Jr., "The Viterbi Algorithm", *Proceedings of the IEEE*, Vol. 61, No. 3, March 1973. Reed-Solomon coding systems are discussed in the Clark, Jr. et al and Lin et al texts cited above.

The error rate performance at the output of the inner, modulation code in concatenated coded systems is highly dependent on signal-to-noise ratio (SNR). Some codes perform better, providing a lower error rate, at a low SNR while others perform better at a high SNR. This means that the optimization of the modulation code for concatenated coding systems can lead to different solutions, depending on the specified SNR range. To date, an optimal solution has eluded system designers.

It would be advantageous to provide an optimized data modulation system with high bandwidth efficiency and low power requirements. Such a system should provide a high data rate, with minimal bandwidth occupancy, and very high data reliability. The complexity of a receiver for use with such a system should be minimized, to provide low cost in volume production.

The present invention provides a modulation system having the aforementioned advantages. In particular, the method and apparatus of the present invention provide a concatenated coding implementation wherein the inner trellis coding rate and the outer Reed-Solomon error correction rate are optimized to provide an integer relationship between the various clocks required by the system (enabling a low cost and easily implemented clock design) while achieving excellent coding gain at a desired symbol rate and bandwidth. The invention achieves very high (e.g., 7 dB) coding gain, requires a very small transmission overhead, and provides a simple scheme for Reed-Solomon synchronization, including Reed-Solomon symbol synchronization, block synchronization, interleave block synchronization, trellis symbol synchronization and frame synchronization. These advantages all combine to provide a very robust system that is low in cost, easy to initialize, and allows synchronization to be easily regained if lost.

SUMMARY OF THE INVENTION

In accordance with the present invention, a method is provided for concatenating an outer symbol error correcting code (e.g., a Reed-Solomon algorithm) with a multidimensional trellis code for use in communicating digital data within a standard (e.g., approximately six MHz) bandwidth television channel. An input signal is encoded using the outer symbol error correcting code to produce successive blocks. Each block comprises N seven-bit coded symbols of which M coded symbols represent information to be communicated and the remaining N-M coded symbols comprise error correcting overhead. M/N is one of 121/127 and

122/128. The symbols in each block are interleaved for transmission in an interleaved order to minimize the effects of burst errors when recovering the input signal after transmission. A seven-bit control symbol is provided for each frame of F blocks, where F=10 when M/N is 122/128 and F=20 when M/N=121/127. The addition of the control symbols effectively lowers the ratio of M/N to an actual information to transmitted data ratio of 120/126=20/21.

The control symbols contain synchronization information necessary to synchronize the recovery of information at a receiver. The blocks are convolutionally encoded using an inner convolutional coding algorithm having a rate 4/5 or 3/4. In this manner, for a sixteen QAM implementation four two-bit output symbols are provided for each seven input bits for each of the I and Q QAM components, and for a sixty-four QAM implementation five three-bit output symbols are provided for each pair of seven-bit (2x7=14 bits) coded symbols. The 3/4 rate for sixteen QAM and 4/5 rate for sixty-four QAM allows for a single or double seven-bit symbol. The two-bit (sixteen QAM) or three-bit (sixty-four QAM) output symbols are multilevel modulated for transmission over a communication path.

The multilevel modulated two or three-bit output symbols are decoded after receipt from a communication path by demodulating them for decoding using a rate 3/4 or 4/5 decoding algorithm to recover the blocks of seven-bit coded symbols and said control symbols. One seven bit coded and/or control symbol is provided for each group of four of the received two-bit output symbols in the sixteen QAM embodiment. Two seven-bit coded and/or control symbols are provided for each group of five of the received three-bit output symbols in the sixty-four QAM embodiment. The recovered blocks are deinterleaved after stripping the control bits therefrom. The seven-bit coded symbols in the deinterleaved blocks are decoded using an algebraic symbol error correcting algorithm that corresponds to the outer symbol error correcting code to recover the input signal. In the illustrated embodiment, the outer symbol error correcting code comprises a Reed-Solomon algorithm and the multilevel modulating step uses either sixteen QAM or sixty-four QAM to modulate the output symbols. The rate 3/4 or 4/5 decoding algorithm is a Viterbi decoding algorithm and the algebraic symbol error correcting algorithm is a Reed-Solomon decoding algorithm.

An encoder is provided in accordance with the invention for concatenating an outer symbol error correcting code with a multidimensional trellis code to efficiently communicate digital data within a standard bandwidth television channel using multilevel modulation. An outer symbol error encoder is provided for encoding an input signal to produce successive data blocks. Each block comprises N seven-bit coded symbols of which M coded symbols represent information to be communicated. The remaining N-M coded symbols comprise error correcting overhead. M/N is one of 121/127 and 122/128. Means are provided for interleaving the symbols in each block for transmission in an interleaved order to minimize the effects of burst errors when recovering the input signal after transmission. A seven-bit control symbol is provided for each frame of F blocks, where F=10 when M/N is 122/128 and F=20 when M/N=121/127. The addition of the control symbols effectively lowers the ratio of M/N to an actual information to transmitted data ratio of 120/126=20/21.

The control symbols contain synchronization information necessary to synchronize the recovery of information at a receiver. A rate 4/5 convolutional encoder is concatenated with the outer symbol error encoder for convolutionally encoding the blocks and control symbols to provide five

three-bit output symbols for two of the seven-bit coded symbols for each of I and Q in a sixty-four QAM embodiment. In a sixteen QAM embodiment, a rate 3/4 encoder provides four two-bit output symbols for each seven bits in a stream of consecutive seven-bit coded symbols. Means are also provided for multilevel modulating the two or three-bit output symbols for transmission over a communication path.

In a preferred embodiment, the outer symbol error encoder comprises a Reed-Solomon encoder. The modulating means comprise one of a sixteen QAM and sixty-four QAM modulator. The convolutional encoder is a trellis encoder.

A decoder is provided for decoding the convolutionally encoded blocks provided by the encoder. The decoder includes means for receiving and demodulating the output symbols from the communication path. An inner decoder is provided for decoding the demodulated output symbols using a rate 3/4 or 4/5 code to recover the blocks of seven-bit coded symbols and the control symbols. Two of the seven-bit coded symbols and/or control symbols are provided for each group of five three-bit output symbols received from the communication path in the sixty-four QAM embodiment. One seven-bit coded symbol or control symbol is provided for each group of four two-bit output symbols received in the sixteen QAM embodiment. Means are provided for deinterleaving the recovered blocks after the control symbols have been stripped therefrom. An outer symbol error decoder is concatenated with the inner decoder for decoding the blocks from the inner decoder to recover the input signal. In a preferred embodiment, the inner decoder is a Viterbi decoder and the outer symbol error decoder is a Reed-Solomon decoder.

A decoder is provided for multilevel modulated digital data communicated in a standard bandwidth television channel. Means are provided for receiving and demodulating convolutionally encoded output symbols from a communication path. An inner decoder is provided for decoding the demodulated output symbols using a rate 3/4 or 4/5 code to recover interleaved blocks of data. Each block comprises N seven-bit coded symbols of which M coded symbols represent information to be recovered. The remaining N-M parity symbols comprise error correcting redundancy. M/N is one of 121/127 and 122/128. The inner decoder also recovers a seven-bit control symbol for each frame F of blocks, where F=10 when M/N is 122/128 and F=20 when M/N is 121/127. The control symbols effectively lower the ratio of M/N to an actual information to transmitted data ratio of 120/126=20/21. Two of the seven-bit coded and/or synchronization symbols are provided for each group of five of the three-bit output symbols received from the communication path in a sixty-four QAM implementation. For sixteen QAM, each group of four two-bit output symbols received provides seven bits for assembly into successive seven-bit coded and/or synchronization symbols.

Means are provided for deinterleaving the recovered blocks after the control symbols have been stripped therefrom. An outer symbol error decoder is concatenated with the inner decoder for decoding the blocks from the inner decoder in response to the control symbols to recover a transmitted information signal. The inner decoder is a Viterbi decoder and the outer symbol error decoder is a Reed-Solomon decoder.

It is possible to implement the present invention in a system where separate control symbols are not necessary to obtain synchronization. For example, synchronization information can be provided as part of the transmitted informa-

tion data. In order to accommodate such a scheme, a method is provided for concatenating an outer symbol error correcting code (e.g., a Reed-Solomon algorithm) with a punctured multidimensional trellis code for use in communicating digital data within an approximately six MHz bandwidth television channel. An input signal is encoded using the outer symbol error correcting code to produce successive blocks. Each block comprises N seven-bit coded symbols of which M coded symbols represent information to be communicated and the remaining N-M coded symbols comprise error correcting overhead. M/N is one of 120/126, 121/127, and 122/128. The symbols in each block are interleaved for transmission in an interleaved order to minimize the effects of burst errors when recovering the input signal after transmission. The blocks are convolutionally encoded using an inner convolutional coding algorithm having a rate 3/4 or 4/5. In this manner, five three-bit output symbols are provided for each pair of seven-bit coded symbols in a sixty-four QAM embodiment. In a sixteen QAM embodiment, four two-bit output symbols are provided for each seven successive bits of the coded input symbols. The two or three-bit output symbols are multilevel modulated for transmission over a communication path.

The multilevel modulated output symbols are decoded after receipt from a communication path using a rate 3/4 or 4/5 decoding algorithm. Two seven-bit coded symbols are provided for each group of five of the received three-bit output symbols in the sixty-four QAM mode and nine successive bits are provided for each group of five of the received two-bit output symbols in the sixteen QAM mode. The recovered blocks are deinterleaved. The coded symbols in the deinterleaved blocks are decoded using an algebraic symbol error correcting algorithm that corresponds to the outer symbol error correcting code to recover the input signal. In the illustrated embodiment, the outer symbol error correcting code comprises a Reed-Solomon algorithm. The rate 3/4 or 4/5 decoding algorithm is a Viterbi decoding algorithm and the algebraic symbol error correcting algorithm is a Reed-Solomon decoding algorithm.

An encoder is provided in accordance with the invention for concatenating an outer symbol error correcting code with a multidimensional trellis code to efficiently communicate digital data within a standard bandwidth television channel using multilevel modulation. An outer symbol error encoder is provided for encoding an input signal to produce successive data blocks. Each block comprises N seven-bit coded symbols of which M coded symbols represent information to be communicated. The remaining N-M coded symbols comprise error correcting overhead. M/N is one of 120/126, 121/127 and 122/128. Means are provided for interleaving the symbols in each block for transmission in an interleaved order to minimize the effects of burst errors when recovering the input signal after transmission. The interleaver can comprise a $2^m/N$ interleaver, where N is an integer from one to six and 2^m represents the maximum burst length to be dispersed. Such an interleaver will spread the burst error over a full block (N) of the seven-bit coded symbols. A rate 3/4 or 4/5 convolutional encoder is concatenated with the outer symbol error encoder for convolutionally encoding the blocks to provide five three-bit output symbols for two of the seven-bit coded symbols (sixty-four QAM) or four two-bit output symbols for every seven bits of the coded symbols (sixteen QAM). Means are also provided for multilevel modulating the output symbols for transmission over a communication path.

In a preferred embodiment, the outer symbol error encoder comprises a Reed-Solomon encoder. The modula-

ing means comprise one of a sixteen QAM and sixty-four QAM modulator. The convolutional encoder is a trellis encoder.

A decoder is provided for decoding the convolutionally encoded blocks provided by the encoder. The decoder includes means for receiving and demodulating the output symbols from the communication path. An inner decoder is provided for decoding the demodulated output symbols using a rate 3/4 or 4/5 code to recover the blocks of seven-bit coded symbols. Means are provided for deinterleaving the recovered blocks. An outer symbol error decoder is concatenated with the inner decoder for decoding the blocks from the inner decoder to recover the input signal. In a preferred embodiment, the inner decoder is a Viterbi decoder and the outer symbol error decoder is a Reed-Solomon decoder.

A decoder is provided for multilevel modulated digital data communicated in a standard bandwidth television channel. Means are provided for receiving and demodulating convolutionally encoded output symbols from a communication path. An inner decoder is provided for decoding the demodulated output symbols using a rate 3/4 or 4/5 code to recover interleaved blocks of data. Each block comprises N seven-bit coded symbols of which M coded symbols represented information to be recovered. The remaining N-M coded symbols comprise error correcting overhead. M/N is one of 120/126, 121/127 and 122/128. Means are provided for deinterleaving the recovered blocks. An outer symbol error decoder is concatenated with the inner decoder for decoding the blocks from the inner decoder to recover a transmitted information signal. In a preferred embodiment, the multilevel modulated digital data is one of sixteen QAM and sixty-four QAM data. The inner decoder is a Viterbi decoder and the outer symbol error decoder is a Reed-Solomon decoder.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a QAM transmission system employing concatenated coding;

FIG. 2 is a block diagram of a trellis encoder in accordance with the present invention;

FIG. 3 is a block diagram of a trellis decoder in accordance with the present invention;

FIG. 4 is a block diagram of the receiver portion of a particular embodiment of the present invention, illustrating the integer relationships between various receiver clock signals; and

FIG. 5 is a diagrammatic illustration of a superframe of blocks provided by an outer symbol error correcting code with inserted control symbols in accordance with the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

FIG. 1 illustrates a concatenated coding system for communicating QAM data. Digital information to be transmitted is input to a symbol error correcting coder 12, such as a Reed-Solomon encoder, via an input terminal 10. Encoder 12 converts the information into a block 14 ("RS Codeword"), comprising a plurality N of successive n-bit coded symbols 16, where n=7. Of the N coded symbols, M represent the actual information to be communicated and the remaining N-M parity symbols comprise error correcting redundancy.

While an outer convolutional code could be used for encoder 12, the bursty nature of the errors in a transmission system, the fact that only hard quantized data is available, and the desirability of a high rate code make a Reed-Solomon code, whose symbols are formed from n-bit segments of the binary stream, a good choice for the outer code. Since the performance of a Reed-Solomon code only depends on the number of symbol errors in the block, such a code is undisturbed by burst errors within an n-bit symbol. However, the concatenated system performance is severely degraded by long bursts of symbol errors. Therefore, an interleaver 18 is provided at the output of Reed-Solomon encoder 12, to interleave the symbols (as opposed to individual bits) between coding operations. The intent of the interleaving is to break up the bursts of symbol errors.

It may be desirable to insert synchronization information into the transmitted data stream. This may be required, for example, where the information data being communicated does not already contain synchronization information. In such a case, after the Reed-Solomon symbols are interleaved, control symbols (which include synchronization symbols) are added via terminal 19 at a rate of one seven-bit control symbol for each frame of Reed-Solomon blocks. In the illustrated embodiments, each Reed-Solomon block comprises either 126, 127 or 128 Reed-Solomon symbols, although the control symbols are only added when blocks of 127 or 128 Reed-Solomon symbols are being processed. A frame comprises F such blocks. Where the blocks contain 128 Reed-Solomon symbols, including 122 information symbols and six parity symbols, F=10. Where each block contains 127 Reed-Solomon symbols, including 121 information symbols and six parity symbols, F=20.

The interleaved Reed-Solomon symbols (with added control symbols, when required) are input to a trellis encoder 20 and QAM modulator 21. The output of modulator 21 comprises symbols representative of coordinates in the real (I) and imaginary (Q) planes of a QAM constellation pattern. One such constellation point 22 is symbolically illustrated in FIG. 1. The symbols are transmitted by a conventional transmitter 24 via a communication channel 26. The communication channel introduces various distortions and delays that corrupt the signal before it is received by a receiver 28. As a result, the coordinate values embodied in the received symbols will not correlate exactly with the transmitted coordinate values, such that a received point 30 will end up on the constellation pattern in a different location than the actual transmitted point 22. In order to determine the correct location for the received point, and thereby obtain the data as actually transmitted, the received data (I, Q) is demodulated in a QAM demodulator 31 and input to a trellis decoder 32 that uses a soft-decision convolutional decoding algorithm to recover the transmitted information. A decoder in accordance with the present invention is described in greater detail below.

The decoded output from decoder 32 is input to a deinterleaver and control symbol stripper 34 that strips out the control symbols (if provided) and reverses the effects of interleaver 18 discussed above. The deinterleaved data is input to a Reed-Solomon decoder 36 for recovery of the original information bits.

FIG. 2 illustrates an encoder in accordance with the present invention. Data bits (e.g., from interleaver 18—FIG. 1) are input to a conventional parsing circuit 42 via an input terminal 40. In accordance with the specific requirements of the sixty-four QAM implementation of the invention, each group of fourteen bits of the interleaved Reed-Solomon data to be transmitted (i.e., two seven-bit Reed-Solomon symbols

for either I or Q) is parsed into ten "uncoded" bits for output on line 44 directly to QAM mapper 50 and four "coded" bits for output on line 46 to a convolutional encoder 48. Convolutional encoder 48 employs a punctured rate 4/5, 16-state trellis code, in which the generators are 25 and 37 in octal. The five bits output from encoder 48 for each four bits input thereto and the ten uncoded bits (fifteen bits total for each fourteen bits of I or Q data input to parsing circuit 42) are presented to the QAM mapper 50 as labels which map to five three-bit symbols for transmission. Thus, the equivalent of two seven-bit Reed-Solomon symbols (fourteen bits total) are transmitted as five three-bit, sixty-four QAM symbols, corresponding to I or Q in the transmitted constellation pattern.

A sixteen QAM implementation is similar, except that parsing circuit 42 provides four uncoded and three coded bits per cycle, such that QAM mapper 50 will receive a total of eight bits total each cycle (four uncoded and four coded after the rate 3/4 convolutional encoder) as labels to map to four two-bit symbols for transmission. Thus, seven bits of the Reed-Solomon symbols are transmitted as four two-bit sixteen QAM symbols, corresponding to I or Q in the transmitted constellation pattern.

FIG. 3 illustrates an implementation of a sixty-four QAM trellis decoder in accordance with the present invention. The received symbol data is input to a pruner 62 via an input terminal 60. Pruner 62 processes the recovered modulation function to provide a set of metrics corresponding to the transmitted coded bits and to provide a plurality of subgroups representing a plurality of conditional determinations of the signal point identified by the transmitted uncoded bits. For each five bits output on line 66 to a rate 4/5 16-state Viterbi decoder 68, four decoded bits are provided at the output of the Viterbi decoder. The conditional determinations of the uncoded bits are output on line 64. The Viterbi decoder 68 can be a rate 1/2 decoder that is punctured to rate 4/5 using well known puncture techniques as disclosed, for example, in Y. Yasuda, et al., "High-Rate Punctured Convolutional Codes for Soft Decision Viterbi Decoding," *IEEE Transactions on Communications*, Vol. COM-32, No. 3, March, 1984, pp. 315-318.

For a sixteen QAM implementation, decoder 68 is replaced with a rate 3/4 decoder. For each four bits output on line 66 to the decoder, three decoded bits are provided. The rate 3/4 decoder can be a rate 1/2 Viterbi decoder punctured to rate 3/4 as well known in the art.

Pruner 62 can comprise a memory device, such as a programmable read only memory (PROM), that stores a look-up table containing precomputed sets of metrics and conditional determinations for different sets of input values (I, Q). The (I, Q) values are used to address the PROM to output the corresponding stored metrics and determinations. This allows a very high speed pruning operation. The Viterbi decoder uses an accumulated history of the metrics received from the pruner to decode the coded bits.

In the embodiment illustrated in FIG. 3, the metrics output from pruner 62 are decoded by decoder 68 to recover a single bit corresponding to each single bit output on line 46 in the encoder of FIG. 2. These bits are reencoded with a rate 4/5 16-state convolutional encoder 70 (identical to encoder 48 in FIG. 2) to recreate the five coded bits corresponding to each set of four coded bits on line 46. The reencoded bits are used by a selector 74 to select hard decisions output from the pruner, after the subgroups have been delayed by a delay buffer 72 for an amount of time equal to the delay introduced by decoder 68. The selected hard decisions are combined

with the recovered bits from decoder 68 in a serializer 76, to provide a trellis decoded output. For the sixteen QAM embodiment, encoder 70 is a rate 3/4 convolutional encoder used to recreate the four coded bits corresponding to each set of three coded bits on line 46.

The decoded output may exhibit a modest symbol error rate that must be further improved by an outer decoder. Thus, further processing of the decoded output, by deinterleaver 34 and a Reed-Solomon outer decoder 36 (FIG. 1) is used to recover the original information bits. An estimate of the output bit error rate, with a given input symbol error rate, for a t error-correcting, Reed-Solomon code can be easily computed in accordance with well known techniques, such as those shown in previously mentioned U.S. Pat. No. 5,233,629.

The present invention provides an optimized combination of concatenated coding for a QAM system. The system parameters include the Reed-Solomon block size M, the number of symbols in a Reed-Solomon block N, and the trellis coding rate p/q. It has been found that the specific combination of N, M, p and q in accordance with the present invention result in substantial and surprising advantages, particularly in the ability to provide improved coding gain, low-cost forward error correction (FEC) and clock circuits, improved symbol rate and bandwidth, a simplified interface with the information clock, and the ability to provide these advantages for both sixty-four QAM and sixteen QAM communication schemes.

The particular parameters provided by the present invention are a Reed-Solomon rate (M/N) of either 120/126 (without added synchronization control symbols), 121/127 or 122/128 with a trellis coding rate (p/q) of 4/5 or 3/4 depending on the QAM level used. This trellis coding rate can be provided by puncturing a standard rate 1/2 trellis code. Use of a convolutional interleaver parameterized by (B, N) is also advantageous, for example where B=32 and is the maximum burst length, and N=128 and is the separation between the interleaved Reed-Solomon blocks. It is noted that in accordance with the present invention, N is also the Reed-Solomon block size (e.g., 128 or 127 seven-bit Reed-Solomon symbols per block).

The specific parameters used in accordance with the present invention provide extremely advantageous relationships between the various clocks used in the encoder and decoder portions of a system for communicating digital data using trellis coded QAM. In one possible implementation, a 5.6 bit per symbol trellis code is combined with a singularly-extended (122, 128) Reed-Solomon code to provide small integer ratios in the clock tree, as follows:

TABLE 1

Signal:	Frequency	Frequency	Relation to Master Clock:	
	for 64 QAM:	for 16 QAM:	(64 QAM)	(16 QAM)
Input Data Clock (f_{data})	8.333 MHz	8.333 MHz	1/6	1/4
QAM Symbol Clock (f_{symbol})	5 MHz	5 MHz	1/16	3/20
System Clock (f_{clock})	80 MHz	33.333 MHz	1	1
Reed Solomon Symbol Clock (f_{RS})	2 MHz	2 MHz	1/40	3/50

It can be seen from Table 1 that for the sixty-four QAM embodiment, the system clock f_{clock} is exactly sixteen times the QAM symbol clock f_{symbol} , exactly six times the input data

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clock f_{info} , and exactly forty times the Reed-Solomon symbol clock f_{RS} . Further, $f_{baud}/f_{info}=3/8$. The use of a rate 4/5 trellis code in order to provide five three-bit output symbols (fifteen bits total) for each pair of seven-bit Reed-Solomon symbols input to the trellis coder (fourteen bits total) enables an integer relationship with the 5.6 bit per symbol trellis code for sixty-four QAM. Specifically, $(f_{clock}/f_{info}) \times (14/15)=5.6$, where $(f_{clock}/f_{info})=6$. The small integer relations (6, 16) between the master clock, input data rate and QAM symbol period make it easy to provide the necessary clocks with a fifty percent duty cycle using a single phase lock loop.

For the sixteen QAM embodiment, f_{clock} is 6% times f_{baud} and four times f_{info} . Further, $f_{baud}/f_{info}=3/5$. The use of a rate 3/4 trellis code in order to provide four two-bit output symbols (eight bits total) for each seven-bit Reed-Solomon symbol input to the trellis coder enables an integer relationship with the 3.5 bit per symbol trellis code. Specifically, $(f_{clock}/f_{info}) \times (7/8)=3.5$, where $(f_{clock}/f_{info})=4$.

In accordance with the present invention, each Reed-Solomon block comprises N seven-bit coded symbols of which M coded symbols represent information to be communicated. The remaining $N-M$ coded symbols comprise error correcting redundancy, specifically parity information. Thus, for a 128 symbol Reed-Solomon block, 122 symbols carry the actual information to be communicated, and the remaining six symbols provide parity information for use at the receiver.

The use of a 121/127 or 122/128 Reed-Solomon rate facilitates the provision of synchronization symbols for use by the receiver in synchronizing the deinterleaver. In these embodiments, a seven-bit control symbol can be inserted for every F Reed-Solomon blocks in synchronization with the interleaver. The control symbols include synchronization symbols for use by the receiver, after being output from the trellis decoder, to determine the start of successive Reed-Solomon blocks and to synchronize the deinterleaver. As an example, where a Reed-Solomon rate of 122/128 is used, one control symbol can be inserted for every 1280 encoded Reed-Solomon symbols ($F=10$). Where a Reed-Solomon rate of 121/127 is used, one control symbol can be added for every 2540 encoded Reed-Solomon symbols ($F=20$). F defines the size (in blocks) of a frame of Reed-Solomon symbols. NF defines the number of symbols per frame. Thus, for a Reed-Solomon rate of 122/128, there are $128 \times 10 = 1280$ symbols per frame. For a Reed-Solomon rate of 121/127, there are $127 \times 20 = 2540$ symbols per frame.

In order for the control symbols to appear in proper order after the trellis decoder, they are inserted in the same symbol position in consecutive frames. It is noted that the sum of the number of blocks in a frame (F) and the number of overhead symbols inserted (S) (i.e., $F+S$) must be divisible by the interleaving depth I . Thus, where N is the Reed-Solomon block size in symbols, and S is the number of synchronization and "pipeline" (i.e., control) symbols:

For 64 QAM:

$$\begin{aligned} f_{info} &= \frac{1}{2} f_{baud} \times \frac{5.6 \text{ bits}}{\text{symbol}} \times \frac{NF}{NF+S} \times \frac{N-6}{N} \\ &= \frac{1}{2} (5) \times 5.6 \times \frac{1280}{1281} \times \frac{122}{128} \\ &= 13.333 \text{ MHz} \end{aligned}$$

For 16 QAM:

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-continued

$$\begin{aligned} f_{info} &= \frac{1}{2} f_{baud} \times \frac{3.5 \text{ bits}}{\text{symbol}} \times \frac{NF}{NF+S} \times \frac{N-6}{N} \\ &= \frac{1}{2} (5) \times 3.5 \times \frac{1280}{1281} \times \frac{122}{128} \\ &= 8.333 \text{ MHz} \end{aligned}$$

F and S can be adjusted as necessary to provide the exact relationship between the input data rate and the QAM symbol period desired for a given Reed-Solomon rate. At the decoder, the control symbols are removed before the symbols from the trellis decoder are input to the Reed-Solomon decoder.

A specific implementation of a plurality of Reed-Solomon blocks with inserted synchronization symbols is illustrated in FIG. 5. In this implementation, a superframe 100 includes six ten-block frames for a total of sixty Reed-Solomon blocks. Each Reed-Solomon block 106, 108 . . . 110 includes an information portion 102 comprising 122 information symbols and a parity portion 104 comprising six parity symbols, for a total 128 Reed-Solomon symbols per block. One control symbol is provided for each frame of ten blocks. Thus, there are a total of six control symbols 112 provided for the six frames (sixty blocks) of Reed-Solomon symbols. This translates into a total of 53,760 Reed-Solomon bits (128×7×60) and forty-two control bits (6×7) per superframe, or 7,686 symbols per superframe.

In a preferred embodiment, of the six control symbols, four are synchronization symbols. The four synchronization symbols provide a 28-bit synchronization pattern for detection 30 at a decoder. Two different 28-bit synchronization patterns are provided. One is used for the I channel and the other is used for the Q channel. The decoder searches for these patterns for use in determining the end of each superframe as well as the channel (I or Q) to which the superframe pertains. The remaining two control symbols in each superframe can be used, for example, to identify whether the system is using sixty-four QAM or sixteen QAM, and for parity.

Additional control symbols can be added, if necessary, by increasing the size of the superframe. For each additional control symbol, another ten-block frame of Reed-Solomon symbols must be added to the superframe.

At the decoder, all of the parity symbols and control symbols are stripped from the superframe before further processing of the information data. Once carrier recovery 45 synchronization is achieved, the trellis decoder resolves the puncture state ambiguity. Then, a search process is undertaken to identify the 28-bit synchronization code. Once this procedure is complete, frame synchronization is achieved by detecting the four seven-bit symbols transmitted every superframe for synchronization. The synchronization pattern is designed to have low correlation to shifted versions of itself on a symbol basis, and to other predictable sections of the incoming waveform, as well known in the art.

The specific implementation of the present invention is particularly adapted for use in the cable television environment. In this environment, the total interference of white noise, unequalsized echoes, phase noise, fixed calculation errors, and all implementation loss is equivalent to 23-24 dB white noise. Under this condition, a sixty-four QAM scheme will generate about 1×10^{-3} probability of symbol errors. In order to achieve a better symbol error performance, such as one error event per fifteen minutes, about seven dB of coding gain is required. The concatenated coding scheme of the present invention provides such gain.

At the receiver, a Viterbi decoder provides soft decisions and good coding gain. The Reed-Solomon decoder further

reduces the probability of symbol errors. The provision of 4/5 or 3/4 trellis coding and 122/128 (or 120/126 or 121/127) Reed-Solomon concatenated coding will provide a coding gain of 7.2 dB for a 16-state Viterbi decoder. For a carrier-to-noise ratio (C/N) of 21.5 dB, the probability of Reed-Solomon block errors is 2×10^{-8} . The concatenated coding provides about 2.5 dB more coding gain than t=5 Reed-Solomon only coding. As noted above, at the rate 4/5 Viterbi decoder, every five symbols (fifteen bits) of input data will generate two symbols (fourteen bits) of Reed-Solomon data in the sixty-four QAM implementation. This simplifies the clock circuit by providing the integer relationships set forth above between the system clock, input data rate and QAM symbol period. The clock of the Reed-Solomon decoder can be derived by dividing the main clock by forty, to arrive at a clock rate of 2.0 MHz. For a rate 3/4 (sixteen QAM) Viterbi decoder, every four symbols (eight bits) of input data will generate one symbol (seven bits) of Reed-Solomon data.

In the system of the present invention, the total transmission rate is 9/8 of the information rate for the sixty-four QAM embodiment and 6/5 of the information rate for sixteen QAM. These ratios further simplify the clock design, allowing for the simple integer relationships mentioned above.

The relationship between the various clock signals in a specific sixty-four QAM embodiment of the invention is illustrated in FIG. 4. This figure illustrates the main components of the symbol decoder provided at a receiver, using a 4/5 rate trellis and a 121/127 Reed-Solomon rate. The master clock 80 operates at a frequency of 80.0 MHz. This clock is divided by six in a divider 88 to generate the 13.333 MHz input data rate, which is used by the Reed-Solomon decoder 92 of the forward error correction unit 94. The QAM symbol period clock, which is one-sixteenth of the master clock (i.e., 5.0 MHz) is applied to the trellis decoder unit 90 of the forward error correction unit 94. Simple relationships are also provided between the master clock frequency and the clocks utilized by the front end sixty-four QAM demodulator 82, back end sixty-four QAM demodulator 84, and the adaptive equalizer 86 of the receiver. Specifically, dividing clock 80 by a factor of four provides the 20.0 MHz clock, dividing by eight provides the 10.0 MHz clock, and dividing by forty provides the 2.0 MHz clock. Similar relationships will result in the sixteen QAM embodiment discussed herein.

It should now be appreciated that the present invention provides an optimal method for concatenating an outer symbol error correcting code with a punctured multidimensional trellis code for use in communicating digital data within an approximately six MHz bandwidth television channel. Encoder and decoder apparatus for effecting the method are also provided. The method and apparatus are particularly useful in communicating digital television signals via a cable television communication path, where low-cost decoders are required. The specific parameters provided in accordance with the present invention for the concatenated coding scheme improve coding gain, reduce the cost of the circuitry by providing simple integer relationships between the various required clocks, and work for both sixty-four QAM and sixteen QAM implementations.

Although the invention has been described in connection with a specific embodiment thereof, those skilled in the art will appreciate that numerous adaptations and modifications may be made thereto without departing from the spirit and scope of the invention as set forth in the claims.

What is claimed is:

1. A method for concatenating an outer symbol error correcting code with a multidimensional trellis code for use in communicating digital data within a standard bandwidth television channel, comprising the steps of:

encoding an input signal using said outer symbol error correcting code to produce successive blocks, each block comprising N seven-bit coded symbols of which M coded symbols represent information to be communicated and the remaining N-M coded symbols comprise error correcting information, wherein an outer symbol error correcting rate M/N is one of rates 120/126, 121/127, and 122/128;

interleaving said N seven-bit coded symbols in said blocks for transmission in an interleaved order to minimize the effects of burst errors when recovering the input signal after transmission;

convolutionally encoding said blocks using a rate 4/5 or 3/4 inner trellis code to provide output symbols; and multilevel modulating the output symbols for transmission over a communication path.

2. A method in accordance with claim 1 wherein said outer symbol error correcting code comprises a Reed-Solomon algorithm.

3. A method in accordance with claim 1 wherein:

said multilevel modulating step modulates said output symbols on I and Q components of a 64 Quadrature Amplitude Modulation constellation; and

said inner trellis code provides five three-bit output symbols from two of said seven-bit coded symbols for modulation on one of said I and Q components.

4. A method in accordance with claim 1 wherein:

said multilevel modulating step modulates said output symbols on I and Q components of a 16 Quadrature Amplitude Modulation constellation; and

said inner trellis code provides four two-bit output symbols from one of said seven bit coded symbols for modulation on one of said I and Q components.

5. A method for decoding the multilevel modulated output symbols provided in accordance with claim 1 comprising the steps of:

receiving and demodulating said output symbols from said communication path;

decoding the demodulated output symbols using a rate 4/5 or 3/4 decoding algorithm to recover said blocks of seven-bit coded symbols;

deinterleaving the recovered blocks; and

decoding the seven-bit coded symbols in the deinterleaved blocks using an algebraic symbol error correcting algorithm that corresponds to said outer symbol error correcting code to recover said input signal.

6. A method in accordance with claim 5 wherein:

said outer symbol error correcting code comprises a Reed-Solomon algorithm;

said multilevel modulating step uses one of 16 Quadrature Amplitude Modulation and 64 to modulate said output symbols;

said decoding algorithm is a Viterbi decoding algorithm; and

said algebraic symbol error correcting algorithm is a Reed-Solomon decoding algorithm.

7. A method in accordance with claim 1 in which said digital information is communicated with control data including synchronization data within said standard bandwidth television channel, comprising the further step of:

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providing a seven-bit control symbol for each frame of ten blocks when said outer symbol error correcting rate M/N is 122/128, the addition of said control symbols effectively lowering M/N to an actual information data to transmitted data ratio of 120/126;

wherein said control symbols are convolutionally encoded with said blocks during said convolutional encoding step.

8. A method for decoding the multilevel modulated output symbols provided in accordance with claim 7 comprising the steps of:

receiving and demodulating said output symbols from said communication path;

decoding the demodulated output symbols using a rate 4/5 or 3/4 decoding algorithm to recover said blocks of seven-bit coded symbols and said control symbols;

stripping said control symbols from said recovered blocks;

deinterleaving the recovered blocks after said control symbols have been stripped therefrom; and

decoding the seven-bit coded symbols in the deinterleaved blocks in response to said control symbols, using an algebraic symbol error correcting algorithm that corresponds to said outer symbol error correcting code to recover said input signal.

9. A method in accordance with claim 1 in which said digital information is communicated with control data including synchronization data within said standard bandwidth television channel, comprising the further step of:

providing a seven-bit control symbol for each frame of twenty blocks when said outer symbol error correcting rate M/N is 121/127, the addition of said control symbols effectively lowering M/N to an actual information data to transmitted data ratio of 120/126.

10. A method for decoding the multilevel modulated output symbols provided in accordance with claim 9 comprising the steps of:

receiving and demodulating said output symbols from said communication path;

decoding the demodulated output symbols using a rate 4/5 or 3/4 decoding algorithm to recover said blocks of seven-bit coded symbols and said control symbols;

stripping said control symbols from said recovered blocks;

deinterleaving the recovered blocks after said control symbols have been stripped therefrom; and

decoding the seven-bit coded symbols in the deinterleaved blocks in response to said control symbols, using an algebraic symbol error correcting algorithm that corresponds to said outer symbol error correcting code to recover said input signal.

11. An encoder for concatenating an outer symbol error correcting code with a multidimensional trellis code to efficiently communicate digital data within a standard bandwidth television channel using multilevel modulation, comprising:

an outer symbol error encoder for encoding an input signal to produce successive data blocks, each block comprising N seven-bit coded symbols of which M coded symbols represent information to be communicated and the remaining $N-M$ coded symbols comprise error correcting overhead, wherein an outer symbol error correcting rate M/N is one of rates 120/126, 121/127, and 122/128;

means for interleaving said N seven-bit coded symbols in said blocks for transmission in an interleaved order to

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minimize the effects of burst errors when recovering the input signal after transmission;

a rate 4/5 or 3/4 trellis encoder concatenated with said outer symbol error encoder for convolutionally encoding said blocks to provide output symbols; and

means for multilevel modulating the output symbols for transmission over a communication path.

12. An encoder in accordance with claim 11 wherein said outer symbol error encoder comprises a Reed-Solomon encoder.

13. An encoder in accordance with claim 11 wherein: said modulating means modulate said output symbols on I and Q components of a 64 Quadrature Amplitude Modulation constellation; and

said trellis encoder provides five three-bit output symbols from two of said seven-bit coded symbols for modulation on one of said I and Q components.

14. An encoder in accordance with claim 11 wherein: said modulating means modulate said output symbols on I and Q components of a 16 Quadrature Amplitude Modulation constellation; and

said trellis encoder provides four two-bit output symbols from one of said seven bit coded symbols for modulation on one of said I and Q components.

15. An encoder in accordance with claim 11 in which said digital information is communicated with control data including synchronization data within said standard bandwidth television channel, further comprising:

means for providing a seven-bit control symbol for each frame of ten blocks when said outer symbol error correcting rate M/N is 122/128, the addition of said control symbols effectively lowering M/N to an actual information data to transmitted data ratio of 120/126; wherein said control symbols are convolutionally encoded with said blocks in said trellis encoder.

16. A decoder for decoding the convolutionally encoded blocks provided by the encoder of claim 15 comprising:

means for receiving and demodulating said output symbols from said communication path;

an inner decoder for decoding the demodulated output symbols using a rate 4/5 or 3/4 code to recover said blocks of seven-bit coded symbols and said control symbols;

means for stripping said control symbols from said recovered blocks;

means for deinterleaving the recovered blocks after said control symbols have been stripped therefrom; and

an outer symbol error decoder concatenated with said inner decoder for decoding the blocks from said inner decoder in response to said control symbols to recover said input signal.

17. An encoder in accordance with claim 11 in which said digital information is communicated with control data including synchronization data within said standard bandwidth television channel, further comprising:

means for providing a seven-bit control symbol for each frame of twenty blocks when said outer symbol error correcting rate M/N is 121/127, the addition of said control symbols effectively lowering M/N to an actual information data to transmitted data ratio of 120/126.

18. A decoder for decoding the convolutionally encoded blocks provided by the encoder of claim 17 further comprising:

means for receiving and demodulating said output symbols from said communication path;

an inner decoder for decoding the demodulated output symbols using a rate 4/5 or 3/4 decoding algorithm to recover said blocks of seven-bit coded symbols and said control symbols;

means for stripping said control symbols from said recovered blocks;

means for deinterleaving the recovered blocks after said control symbols have been stripped therefrom; and an outer symbol error decoder concatenated with said inner decoder for decoding the blocks from said inner decoder in response to said control symbols to recover said input signal.

19. A decoder for decoding the convolutionally encoded blocks provided by the encoder of claim 11 comprising:

means for receiving and demodulating the output symbols from said communication path;

an inner decoder for decoding the demodulated output symbols using a rate 4/5 or 3/4 code to recover said blocks of seven-bit coded symbols;

means for deinterleaving the recovered blocks; and

an outer symbol error decoder concatenated with said inner decoder for decoding the blocks from said inner decoder to recover said input signal.

20. A decoder in accordance with claim 19 wherein:

said outer symbol error encoder comprises a Reed-Solomon encoder;

said modulator is one of a 16 Quadrature Amplitude Modulation and 64 Quadrature Amplitude Modulation 30 modulator;

said inner decoder is a Viterbi decoder; and

said outer symbol error decoder is a Reed-Solomon decoder.

21. An encoder in accordance with claim 11 wherein said interleaver means comprise a $2^n/N$ interleaver, where n is an integer from 1 to 6 and 2^n represents a maximum burst length to be dispersed over the N seven-bit coded symbols in one of said blocks.

22. A decoder for multilevel modulated digital data communicated in a standard bandwidth television channel comprising:

means for receiving and demodulating convolutionally encoded output symbols from a communication path; an inner decoder for decoding the demodulated output symbols using a rate 4/5 code to recover interleaved blocks of data, each block comprising N seven-bit coded symbols of which M coded symbols represent information to be recovered and the remaining $N-M$ coded symbols comprise error correcting overhead, wherein an outer symbol error correcting rate M/N is one of rates 120/126, 121/127, and 122/128;

means for deinterleaving the recovered blocks; and

an outer symbol error decoder concatenated with said inner decoder for decoding the blocks from said inner decoder to recover a transmitted information signal.

23. A decoder in accordance with claim 22 wherein:

said multilevel modulated digital data is one of 16 Quadrature Amplitude Modulation and 64 Quadrature Amplitude Modulation data;

said inner decoder is a Viterbi decoder; and

said outer symbol error decoder is a Reed-Solomon decoder.

24. A decoder in accordance with claim 22 wherein:

said outer symbol error correcting rate M/N is either 122/128 or 121/127;

said inner decoder also recovers a seven-bit control symbol for each frame of F blocks, where $F=10$ when M/N is 122/128 and $F=20$ when M/N is 121/127, said control symbols effectively lowering M/N to an actual information data to transmitted data ratio of 120/126; and said deinterleaving means deinterleave the recovered blocks after stripping said control symbols therefrom.

25. A decoder in accordance with claim 24 wherein:

said multilevel modulated digital data is one of 16 Quadrature Amplitude Modulation and 64 Quadrature Amplitude Modulation data;

said inner decoder is a Viterbi decoder; and

said outer symbol error decoder is a Reed-Solomon decoder.

* * * * *

EXHIBIT B



US005621761A

United States Patent [19]**Heegard****Patent Number: 5,621,761****Date of Patent: Apr. 15, 1997**

[54] **ROTATIONALLY INVARIANT TRELLIS CODING INCORPORATING TRANSPARENT BINARY CONVOLUTIONAL CODES**

[75] Inventor: Chris Heegard, Ithaca, N.Y.

[73] Assignee: General Instrument Corporation of Delaware, Chicago, Ill.

[21] Appl. No.: 353,064

[22] Filed: Dec. 9, 1994

[51] Int. Cl.⁶ H04L 5/12; H04L 23/02

[52] U.S. Cl. 375/265; 375/262; 375/341; 371/43; 341/51; 341/106

[58] Field of Search 375/262, 265, 375/341; 371/43; 341/51, 106

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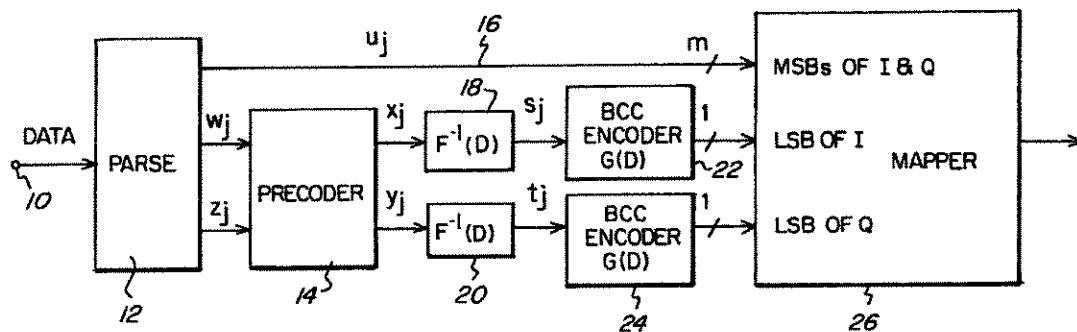
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5,396,518	3/1995	How	375/265
5,535,228	7/1996	Dong et al.	375/265

*Primary Examiner—Stephen Chin
Assistant Examiner—Don Vo
Attorney, Agent, or Firm—Barry R. Lipsitz; Ralph F. Hoppin*

[57] **ABSTRACT**

A rotationally invariant trellis coder is provided for encoding data to be transmitted using a two-dimensional symbol modulation. A precoder, provided at the transmitter, processes data such that a counterpart postcoder at the receiver will provide an output that is invariant to any multiple of a 90° rotation. An encoder encodes the precoded data using a transparent binary convolutional code, which can be a punctured or unpunctured code. The encoded data is mapped to a two-dimensional signal space having a plurality of signal points. The signal points are labeled with unique binary codes in which the two least significant bits, denoted by (I_j, Q_j) , are permuted and partially complemented to (\bar{Q}_j, \bar{I}_j) for each 90° phase rotation around the signal space. The remaining most significant bits for each point, if any, are invariant to such rotation. The postcoder provided at the receiver inverts the precoder and is feedback-free, thus limiting error propagation.

27 Claims, 6 Drawing Sheets



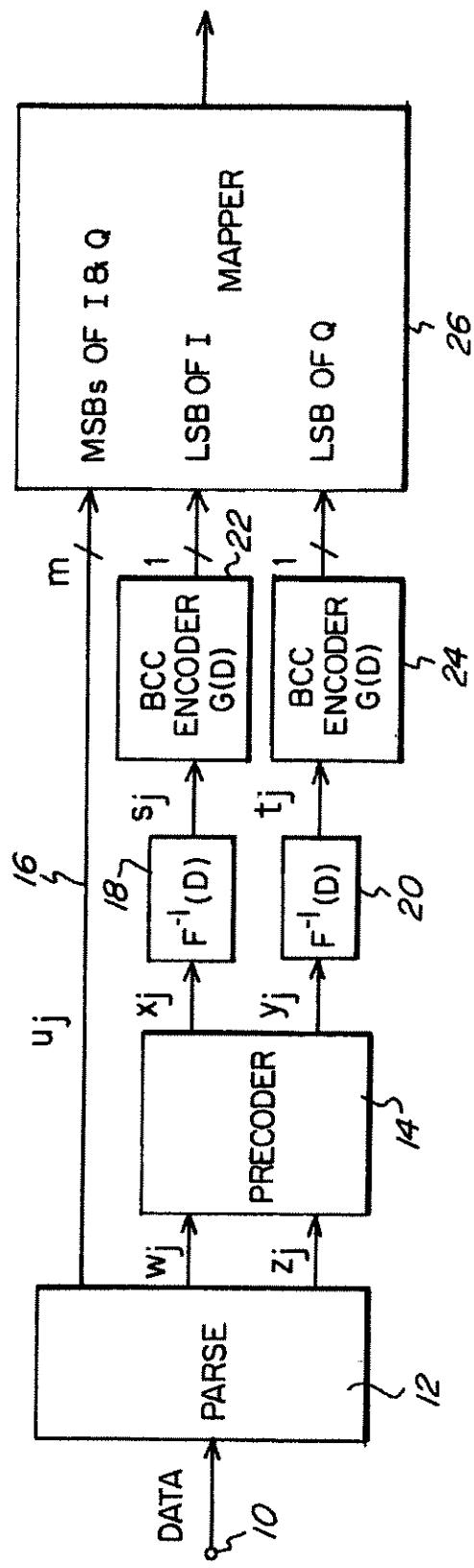


FIG. 1

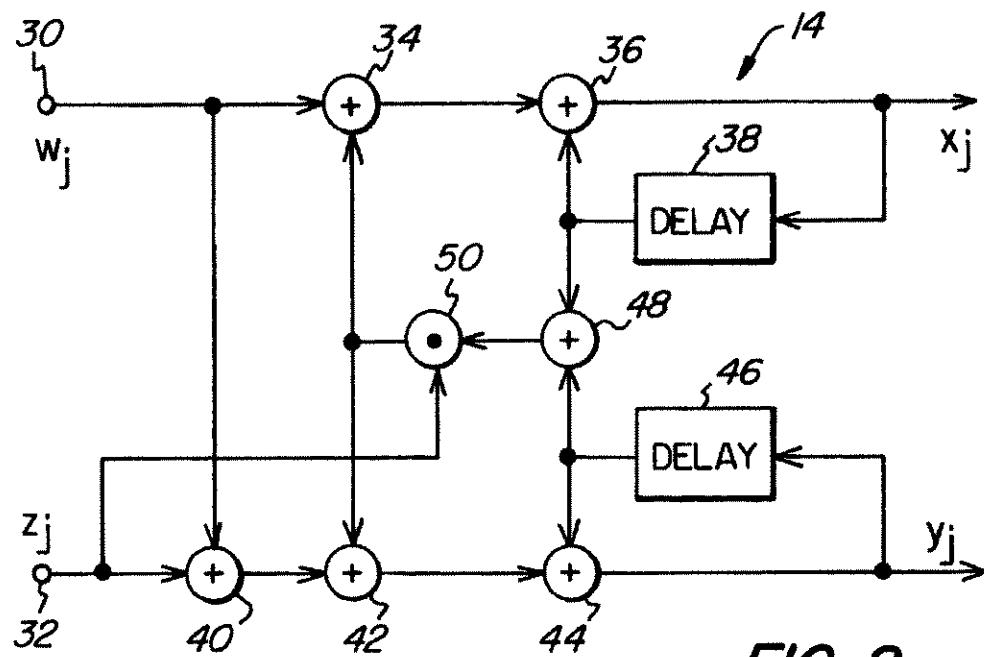


FIG. 2

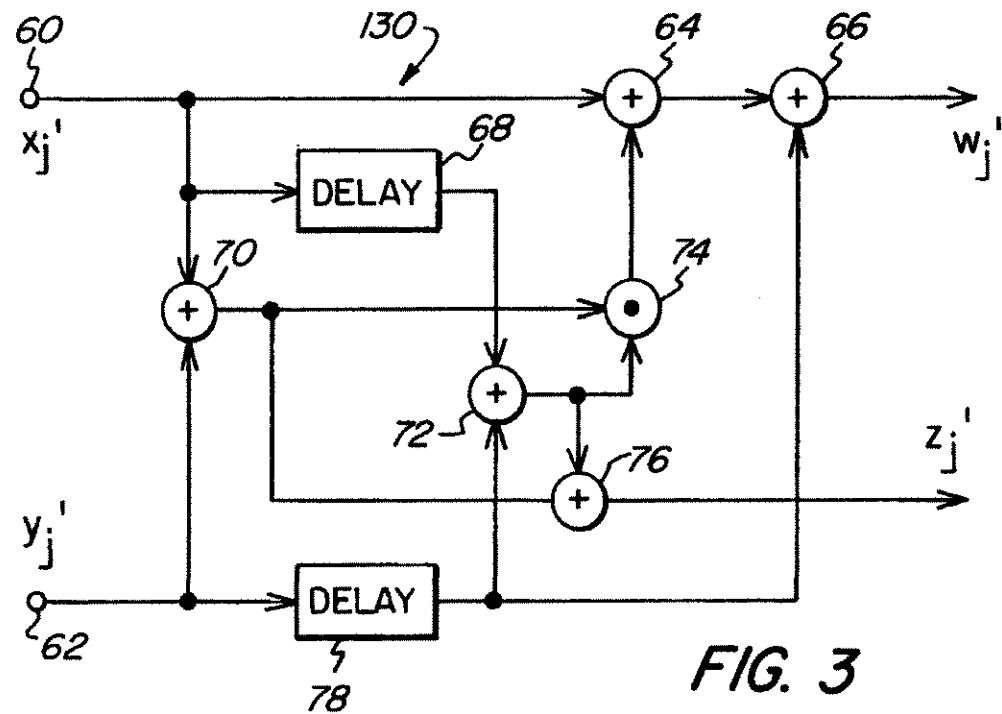


FIG. 3

QPSK

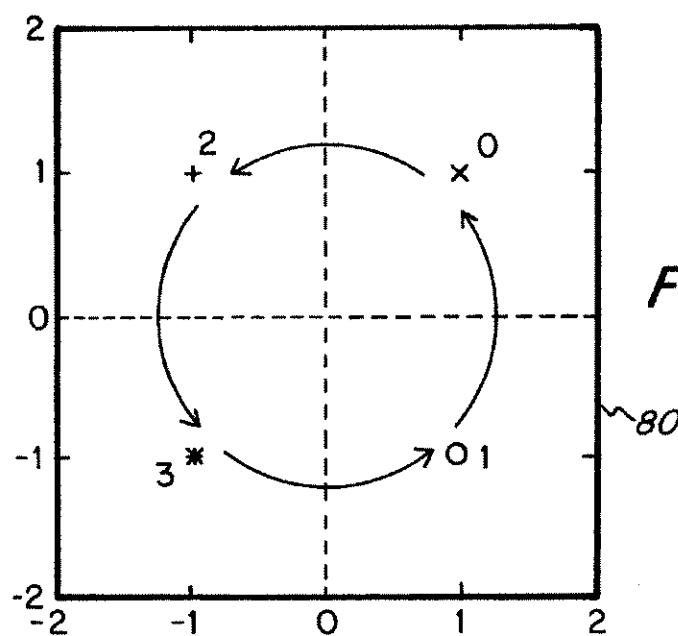


FIG. 4

16 QAM

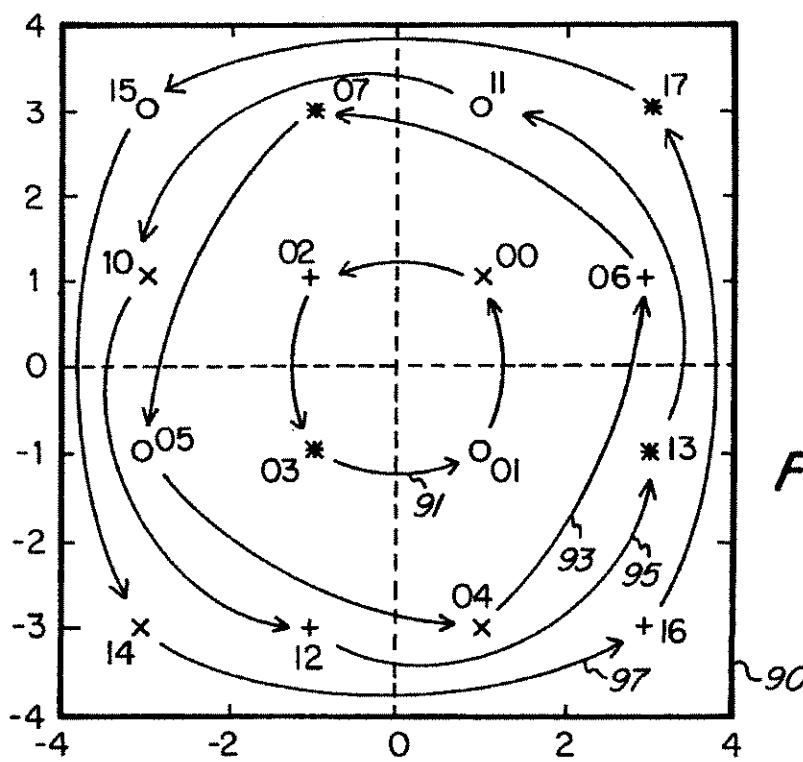


FIG. 5

64 QAM

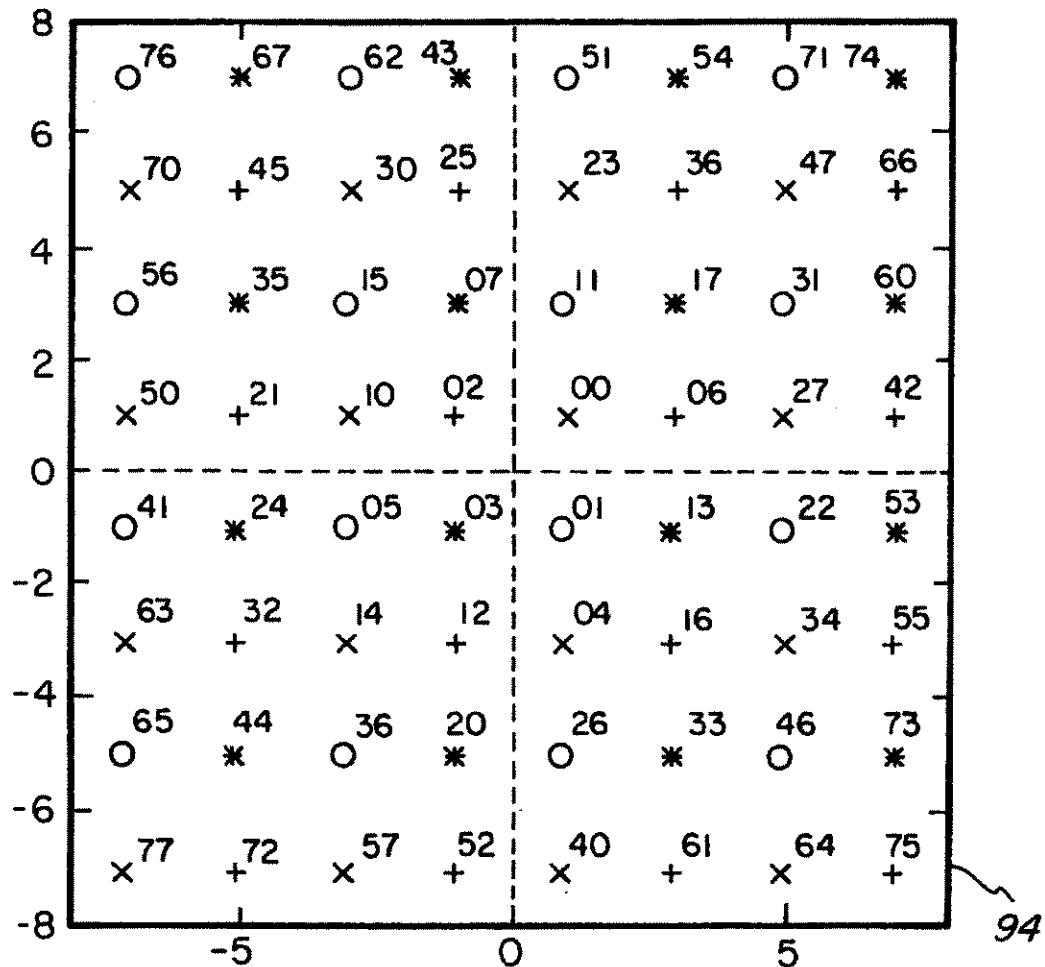


FIG. 6

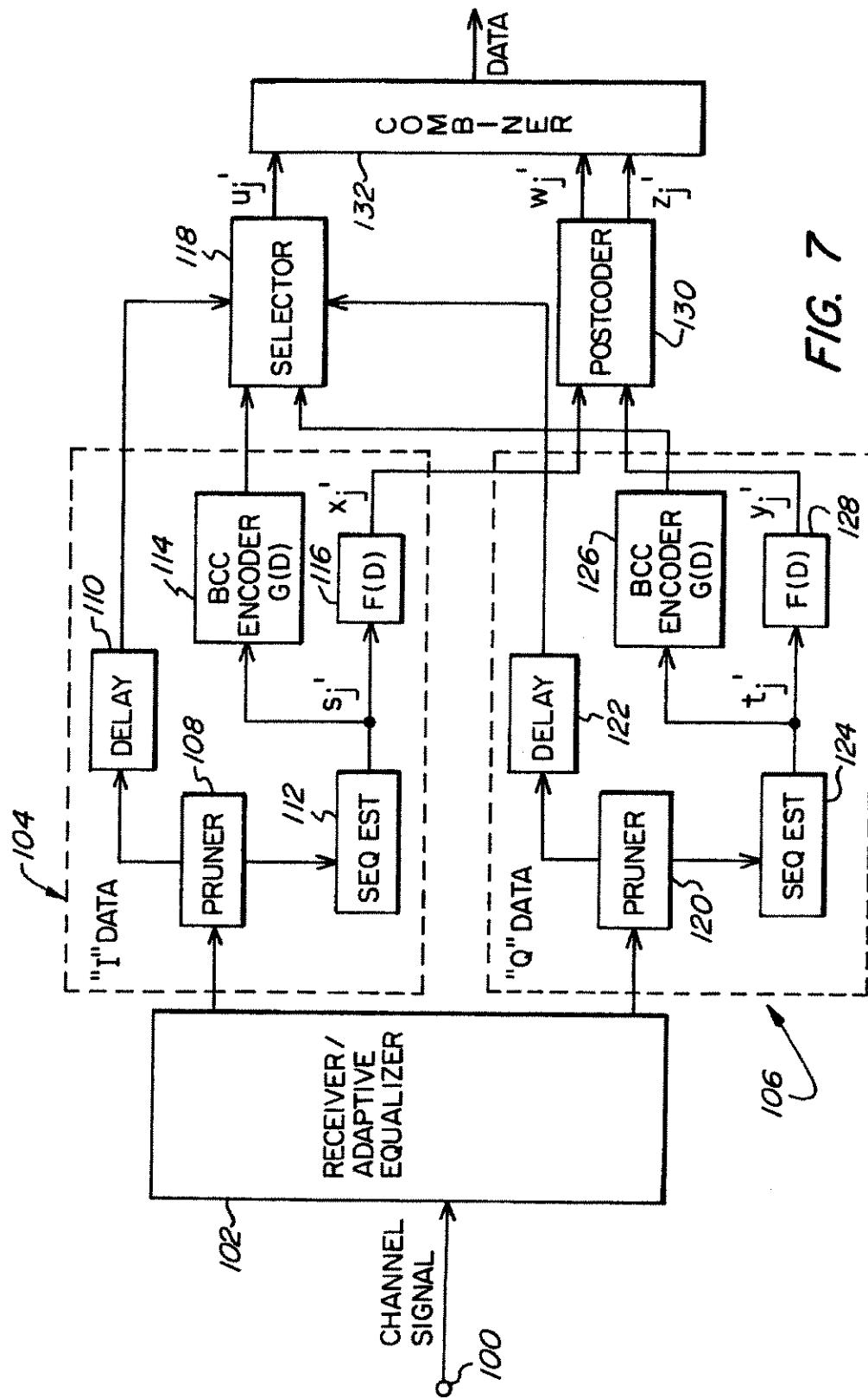


FIG. 7

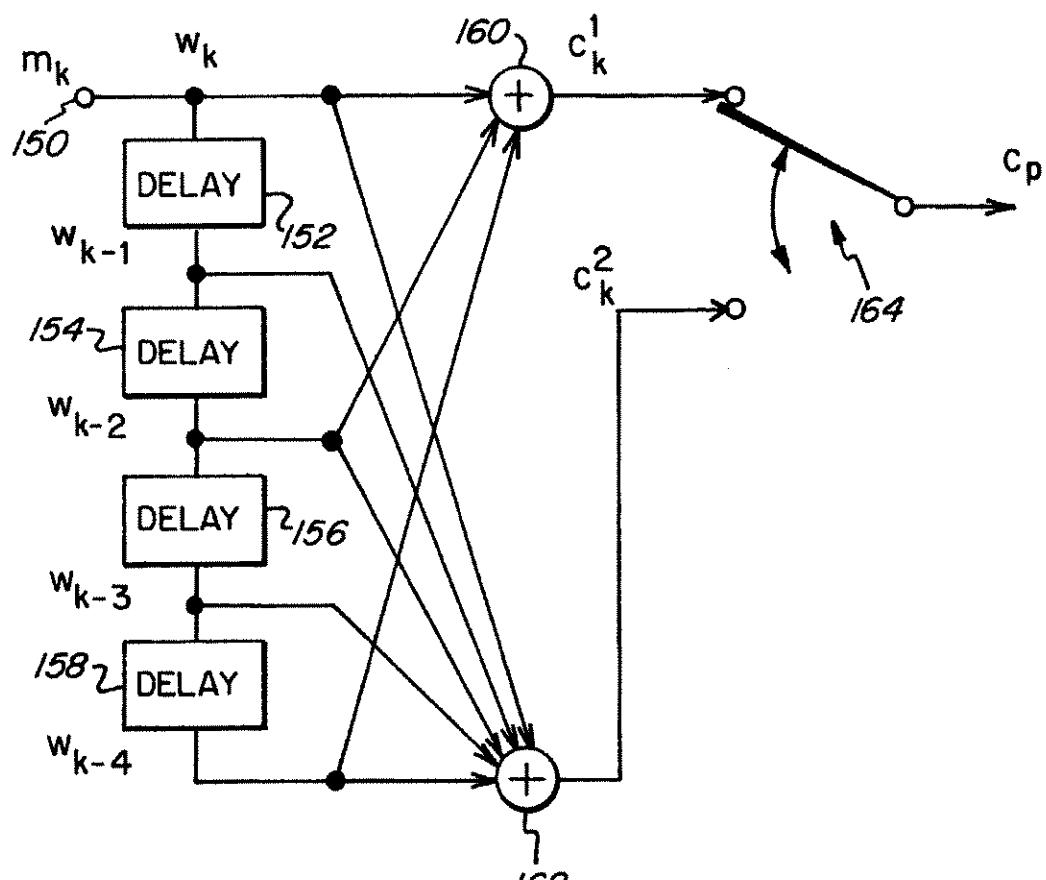


FIG. 8

**ROTATIONALLY INVARIANT TRELLIS
CODING INCORPORATING TRANSPARENT
BINARY CONVOLUTIONAL CODES**

BACKGROUND OF THE INVENTION

The present invention relates to the communication of digital data using trellis coded modulation, and more particularly to a method and apparatus for incorporating a rotationally invariant trellis encoding/decoding scheme into a quadrature phase shift keyed (QPSK) or quadrature amplitude modulation (QAM) transmission system. One of the various applications for which the present invention is particularly well suited is in the transmission of digital television signals.

Digital data, for example, digitized, compressed television (NTSC) or high-definition television (HDTV) signals can be transmitted over terrestrial very high frequency (VHF), ultra-high-frequency (UHF), satellite channels or cable television analog channels to end users. In order to communicate digital data via an analog channel, the data is modulated using, for example, a form of pulse amplitude modulation (PAM). Typically, quadrature amplitude modulation (QAM) or single-sideband (SSB) modulation is chosen to efficiently use the available channel bandwidth. QAM is a quadrature, or orthogonal combination of two PAM signals. When viewed as coordinates of a plane, the combined PAM signals form a signal space or "constellation" of possible transmission levels. Each transmitted constellation point is called a symbol. For example, two independent, quadrature four-level AM signals form a 16-QAM constellation which encodes four bits. A 32-point constellation can be formed with dependent six-level AM quadrature signals, encoding five bits per symbol. In systems that have a lower carrier-to-noise ratio (CNR) than can be tolerated by QAM, lower modulation orders are useful, such as QPSK having a four-point constellation.

In pulse amplitude modulation, each signal is a pulse whose amplitude level is selected from a fixed set of levels. In 16-QAM, each of the quadrature PAM signals select from uniformly spaced, bipolar amplitudes scaled from amplitude levels -3, -1, 1, 3. Spectral efficiency in digital communication systems is defined as the number of transmitted information bits per second per unit of bandwidth, i.e., the ratio of the data rate to the bandwidth. Modulation systems with very high bandwidth efficiency are employed in applications that require high data throughput with small available bandwidth. QAM and SSB provide bandwidth efficient modulation, which can provide very low bit error rates when used with high efficiency forward error correction codes such as trellis coded modulation (TCM).

Trellis coded modulation has evolved as a combined coding and modulation technique for digital transmission over bandlimited channels. Unlike the traditional application of convolutional codes to two-level PAM, which increases the bandwidth used in transmission, TCM increases the constellation size instead. In TCM schemes, a sequence of "coded" bits are convolutionally encoded into a sequence of groups which partition the symbol constellation. For each encoded group of a QAM constellation, a number of "uncoded" bits are transmitted by selecting a unique constellation element of the group. Most TCM schemes map one step of the convolutional code trellis to one transmission symbol which consists of two QAM components (I, Q). Such two-dimensional (2-D) codes achieve a throughput of an integer number of information bits per 2-D symbol.

At a receiver, the sequence of transmitted groups is decoded by a soft-decision maximum likelihood (ML) convolutional code decoder. Such TCM schemes can improve the robustness of digital transmission against additive noise by three to six dB or more, compared to uncoded modulation at the same information rate. One widely used technique for efficient ML decoding of convolutional codes is the Viterbi algorithm disclosed in A. J. Viterbi and J. K. Omura, *Principles of Digital Communications and Coding*, New York, N.Y., McGraw Hill 1979. It is known that decoding of high-rate R convolutional codes can be simplified by using "punctured" codes, which are obtained by periodically deleting some of the output bits of a lower rate code. A rate 1/n code can be punctured to a rate m/k and can be easily decoded with simple modifications to a rate 1/n decoder. An example of such a decoder is provided in commonly assigned, copending U.S. patent application Ser. No. 08/054, 642 filed on May 5, 1993 for "Apparatus and Method for Communicating Digital Data Using Trellis Coding with Punctured Convolutional Codes."

Fast recovery from phase ambiguities is very important for robust modem design. Of all the tracking loops in a typical receiver, such as the automatic gain control, adaptive equalizer, and carrier timing loop, the carrier recovery loop is often the most fragile, resulting in noise. Phase ambiguities can cause a carrier timing slip, requiring a major resynchronization of the forward error correction (FEC), leading to a burst of errors at the FEC output. The Viterbi algorithm (or other sequence estimator used) must detect the event and restart the decoding. Therefore, it would be desirable to provide a coding method that quickly recovers from a phase rotation without causing the FEC to change state. Such a coding method would be particularly useful in the design of a receiver that can cancel large amounts of phase noise introduced in the mixing process.

To robustly track phase jitter, the carrier timing loop bandwidth is typically opened, causing the signal-to-noise ratio (SNR) in the loop to degrade. This leads to exposure to phase flips, limiting the ability of the receiver to handle phase noise. Quick recovery from carrier timing loop slips enables a more aggressive phase noise cancellation to be implemented without the risk of a large error burst appearing at the output of the FEC.

One problem that has been encountered with multilevel modulation techniques, particularly when used with trellis coding, is that 90° phase ambiguities may occur in the signal received from a communication channel. Such phase ambiguities make it difficult to determine the absolute phase of the symbol that has been received. Decoding errors will occur when incorrect assumptions are made as to whether one point or another point in the same group, but offset by 90°, has been received.

It would be advantageous to provide a rotationally invariant trellis encoding/decoding scheme for use in a QPSK or QAM transmission system or the like. Such a scheme should resolve all multiples of 90° phase ambiguities. Quick recovery from phase flip in a receiver should be provided. Any propagation of errors should be insignificant, and coding gain should not be adversely affected.

The present invention provides a rotationally invariant trellis encoding/decoding scheme enjoying the aforementioned advantages.

SUMMARY OF THE INVENTION

In accordance with the present invention, a rotationally invariant trellis coder is provided for encoding input data to

be transmitted to a receiver using a two-dimensional symbol modulation. A precoder is provided for processing said input data. The precoder comprises nonlinear logic that is the inverse of logic provided by a counterpart postcoder at said receiver. An encoder encodes the precoded data using a transparent binary convolutional code, which can be a punctured code. Means are provided for mapping the encoded data from the encoder to a two-dimensional signal space having a plurality of signal points. The signal points are labeled with unique binary codes in which the two least significant bits, denoted by (I, Q), are permuted and partially complemented to (Q, I) for each 90° phase rotation around the signal space. The remaining most significant bits for each point, if any, are invariant to such rotation.

In an illustrated embodiment, the precoder converts a first input data stream w_j and a second input data stream z_j data to corresponding precoded data streams x_j and y_j , respectively, using feedback of delayed data x_{j-1} and y_{j-1} in accordance with the relationships:

$$x_j = w_j \oplus x_{j-1} \oplus z_j \odot (x_{j-1} \oplus y_{j-1}).$$

and

$$y_j = z_j \oplus w_j \oplus y_{j-1} \oplus z_j \odot (x_{j-1} \oplus y_{j-1}).$$

The x_j and y_j data streams output from the precoder are convolutionally encoded to provide the two least significant bits of symbols that are mapped to the signal points in the signal space. In a QAM embodiment, as opposed to a QPSK embodiment, uncoded bits are provided in addition to the coded bits. Means are provided for parsing the uncoded bits from the input data for use by the mapping means. The uncoded bits represent the most significant bits of the symbols that are mapped to the signal points in the signal space.

A decoder is provided for use in decoding symbols output from the trellis coder. At least one sequence estimator, such as a Viterbi algorithm, is used to recover the precoded data from a received data stream. A postcoder is provided for receiving and processing the recovered precoded data to provide output data that is invariant to 90° rotations of the recovered precoded data.

In order to accommodate QAM data, means can be provided in the decoder for pruning the received data stream to recover coded and uncoded bits therefrom. The coded bits are input to the sequence estimator. Means are provided for selecting uncoded in-phase (I) data or uncoded quadrature phase (Q) data for combination with the postcoded data from the postcoder. The precoded data recovered by the sequence estimator is reencoded for use in actuating the selecting means to select the uncoded I data or the uncoded Q data.

Where the precoder converts a first input data stream w_j and a second input data stream z_j to corresponding precoded data streams x_j and y_j , respectively, as set forth above, the postcoder will convert the precoded data recovered from the data streams, namely x_j' and y_j' , respectively, to a first output data stream w_j' and a second output data stream z_j' in accordance with the relationships:

$$w_j' = x_j' \oplus y_{j-1}' \oplus (x_j \oplus y_j) \odot (x_{j-1} \oplus y_{j-1}).$$

and

$$z_j' = y_j \oplus x_j \oplus y_{j-1} \oplus x_{j-1}'.$$

The invention also provides a precoder for use in a rotationally invariant trellis coder. A first path of the pre-

coder has a plurality of exclusive OR gates for converting a first input data stream w_j to corresponding precoded data x_j . A second path has a plurality of exclusive OR gates for converting a second input data stream z_j to corresponding precoded data y_j . A first feedback path is coupled to obtain the precoded data x_j from the first path. The first feedback path includes delay means for providing previous data x_{j-1} . A second feedback path is coupled to obtain the precoded data y_j from the second path. The second feedback path includes delay means for providing previous data y_{j-1} . The first and second feedback paths have at least one common exclusive OR gate and at least one common AND gate. The precoder converts the first and second input data streams to the precoded data in accordance with the relationships:

$$x_j = w_j \oplus x_{j-1} \oplus z_j \odot (x_{j-1} \oplus y_{j-1}),$$

and

$$y_j = z_j \oplus w_j \oplus y_{j-1} \oplus z_j \odot (x_{j-1} \oplus y_{j-1}).$$

A postcoder for use in a rotationally invariant trellis decoder is also provided. The postcoder includes a first path having a plurality of exclusive OR gates for providing an output data stream w_j' from a received precoded data stream x_j' recovered using a sequence estimation algorithm, such as a Viterbi algorithm. A second path has a plurality of exclusive OR gates for providing an output data stream z_j' from a received precoded data stream y_j' recovered using the sequence estimation algorithm. An AND gate has a first input coupled to receive the exclusive OR of the precoded data streams x_j' and y_j' from the first and second paths, respectively. A second input of the AND gate is coupled to receive the exclusive OR of delayed data streams x_{j-1}' and y_{j-1}' from the first and second paths, respectively. The AND gate has an output coupled to an input of one of the exclusive OR gates in the first path. The postcoder produces the output data streams w_j' and z_j' from the precoded data streams x_j' and y_j' in accordance with the relationships:

$$w_j' = x_j' \oplus y_{j-1}' \oplus (x_j \oplus y_j) \odot (x_{j-1} \oplus y_{j-1}),$$

and

$$z_j' = y_j \oplus x_j \oplus y_{j-1} \oplus x_{j-1}'.$$

A method is provided for coding digital data to enable rotationally invariant trellis coded modulation thereof. A stream of bits to be coded is first precoded to render them rotationally invariant when encoded with a transparent binary convolutional code and subsequently decoded and postcoded at a receiver. The precoded bits are encoded using the transparent binary convolutional code to provide coded information. The coded information is mapped to a two-dimensional signal space having a plurality of signal points. The signal points are labeled with unique binary codes in which the two least significant bits, denoted by (I, Q), are permuted and partially complemented to (Q, I) for each 90° phase rotation around the signal space. The remaining most significant bits for each point, if any, are invariant to such rotation.

The coded information provided by the method of the invention can be representative of in-phase (I) and quadrature phase (Q) data. The I and Q data are transmitted over a communication channel in accordance with the signal space mapping. The I and Q data are received from the communication channel and demodulated. The coded information for the I and Q data is decoded to recover the precoded bits. The recovered precoded bits are postcoded to reverse the

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effect of the precoding step in order to recover the stream of bits.

When the method is used for QAM transmission, the data is parsed prior to the precoding step into a stream of uncoded bits and the stream of bits to be coded. The uncoded bits are mapped to the most significant bits of signal points in the signal space. The coded information derived from the stream of bits to be coded is mapped to the least significant bits of the signal points. The uncoded bits and coded information can represent in-phase and quadrature phase data. The I and Q data are transmitted over a communication channel in accordance with the signal space mapping. The I and Q data are received from the communication channel and demodulated. The demodulated I data is pruned to recover corresponding uncoded bits and coded information. The demodulated Q data is also pruned to recover corresponding uncoded bits and coded information. The pruned coded information for the I and Q data is decoded to recover the precoded bits. The recovered precoded bits are postcoded to recover the stream of bits that was coded at the encoder. The recovered precoded bits are reencoded using the transparent binary convolutional code to provide control signals. Uncoded bits pruned from the I data or from the Q data are selected in response to the control signals for combination with the stream of bits recovered by the postcoding step in order to reconstruct the digital data.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a rotationally invariant encoder in accordance with the present invention;

FIG. 2 is an illustrative embodiment of a precoder that can be used in the encoder of FIG. 1;

FIG. 3 is an illustrative embodiment of a postcoder that can be used in a decoder for signals received from the encoder of FIG. 1;

FIG. 4 is a constellation diagram for a QPSK implementation in accordance with the present invention;

FIG. 5 is a constellation diagram for a 16-QAM embodiment in accordance with the present invention;

FIG. 6 is a constellation diagram for a 64-QAM embodiment in accordance with the present invention;

FIG. 7 is a block diagram of a decoder in accordance with the present invention; and

FIG. 8 is a block diagram of a binary convolutional code encoder that can be used in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a method and apparatus for incorporating a rotationally invariant trellis encoding scheme into a two-dimensional symbol (e.g., QPSK or QAM) transmission system subject to a 90° phase ambiguity. The method of coding involves the use of a transparent binary convolutional code and a two-dimensional signal space mapping in conjunction with a precoding and postcoding function. The method is compatible with any transparent binary convolutional code, including punctured codes. An example of such a code is the 64-state code described in J. A. Heller and I. M. Jacobs, "Viterbi Decoding for Satellite and Space Communication," *IEEE Trans. Commun. Technol.*, COM-19, pp. 835-848, October 1971.

Rotationally invariant (RI) trellis codes with RI encoders/uncoders are highly desirable as a method of handling 90° phase ambiguities in transmission systems such as QPSK and QAM. The coding method of the present invention utilizes a transparent binary convolutional code. A binary convolutional code (BCC) is said to be transparent if the complement of any codeword is always a codeword. Since BCCs are linear codes, a BCC is transparent if and only if the "all 1's" sequence is a codeword. For an (n, k) BCC described by a generator matrix G(D) (a $k \times n$ polynomial matrix of rank k) and a parity check matrix H(D) (a $n - (k \times n)$ polynomial matrix of rank $n - k$, $G(D)H(D)^T = 0$), the code is transparent if and only if the sum of the columns of H(D) is divisible by 1-D.

A rotationally invariant code always has a rotationally invariant encoder/decoder. Such an encoder/decoder has the property that the output of the uncoder for any codeword is the same as the output when the codeword is first rotated by 0°, 90°, 180° or 270° before being presented to the uncoder. In other words, a codeword and rotated version thereof produce the same output at the uncoder. Such an uncoder is required to be feedback-free as, for example, in a finite impulse response (FIR) filter, to ensure finite error propagation at the receiver, while the encoder has feedback as, for example, in an infinite impulse response (IIR) filter.

The transparent binary convolutional code is mapped to a two-dimensional signal space which is uniquely labeled. In particular, counterpart symbols in successive symbol groups are labeled with least significant bits (I, Q) such that under counterclockwise 90° rotation, the LSBs will be permuted and partially complemented to (\bar{Q}, I). For a QPSK constellation, if the two bits labeling the four points are denoted by (I_j, Q_j), then

$$(I_j, Q_j) \rightarrow (\bar{Q}_j, I_j) \rightarrow (\bar{I}_j, \bar{Q}_j) \rightarrow (Q_j, \bar{I}_j) \rightarrow (I_j, Q_j).$$

The key to this mapping is that under 90° rotation,

$$(I_j, Q_j) \rightarrow (\bar{Q}_j, I_j)$$

FIG. 1 illustrates an encoder in accordance with the present invention. Serial data to be encoded is input via terminal 10 to a parser 12, which in the case of modulation levels higher than QPSK (e.g., QAM) parses the data into uncoded bits u_j output on path 16 to mapper 26 and a first data stream (w_j) as well as a second data stream (z_j) that are input to a precoder 14. The precoder 14 precodes the data streams (w_j, z_j) to render the data represented thereby rotationally invariant at a receiver when properly encoded and mapped at the encoder and decoded and postcoded at the receiver. The precoded data output from precoder 14 (x_j, y_j) is input to optional feedback matrices 18, 20, respectively. The two binary outputs of the precoder are independently encoded with separate binary convolutional encoders 22, 24. The BCC outputs, along with the remaining uncoded information u_j on line 16 are combined to select the QAM constellation point to be transmitted. It should be appreciated that in a QPSK implementation, there are no uncoded bits and line 16 is not necessary.

The mapping of the BCC outputs is such that they independently select the least significant bit (LSB) of the "I" and "Q" coordinates. In addition, the uncoded or "parallel edge" information u_j is rotationally invariant.

The encoding of the transparent code described by the polynomial generator matrix G(D) is accomplished by the optional feedback matrix $F^{-1}(D)$ followed by the feedforward generator G(D). This structure allows for various encoders for the selected code. For example, a "systematic"

encoder is possible. The only requirement on the encoder matrices is that if the input to $G(D)$ (or $F^{-1}(D)$) is complemented such that zeros become ones, and vice versa, then the output is complemented. This is always possible for a transparent BCC.

The precoder 14 has a structure that results in rotational invariance when combined with a transparent BCC and the aforementioned rotationally invariant labeling of the signal set (described in greater detail below in connection with FIGS. 4-6). In the preferred embodiment, the precoder converts the w_j and z_j data to corresponding precoded data x_j and y_j , respectively, using feedback of delayed data x_{j-1} and y_{j-1} in accordance with the relationships:

$$x_j = w_j \oplus x_{j-1} \oplus z_j \odot (x_{j-1} \oplus y_{j-1}),$$

and

$$y_j = z_j \oplus w_j \oplus y_{j-1} \oplus z_j \odot (x_{j-1} \oplus y_{j-1}),$$

in which the symbol \oplus represents an exclusive OR operation and the symbol \odot represents an AND operation.

A counterpart postcoder is necessary at the decoder, described in greater detail below in connection with FIG. 7. The postcoder converts the precoded data x_j' and y_j' recovered from a communication channel to respective w_j' and z_j' data in accordance with the relationships:

$$w_j' = x_j \oplus y_{j-1} \oplus (x_j \oplus y_j) \odot (x_{j-1} \oplus y_{j-1}),$$

and

$$z_j' = y_j \oplus x_j \oplus y_{j-1} \oplus x_{j-1}.$$

The x_j , y_j , w_j , and z_j terms are primed in the postcoder equations merely to represent that they may be nonidentical to the corresponding terms at the precoder, due to (1) errors introduced in the communication channel and (2) a phase discrepancy of 90°, 180° or 270° between the absolute phase of the transmitter and receiver. Ideally, however, up to the phase discrepancy, these terms would be identical at both the precoder and postcoder.

It can be seen from the above relationships that (1) the postcoder inverts the precoder, (2) the output of the postcoder is the same under the map $(x_j, y_j) \rightarrow (\bar{y}_j, \bar{x}_j)$ (or any integer power of this map), and (3) the postcoder function is feedback-free (i.e., it represents a "sliding window" function of its input) and thus limits error propagation.

A preferred implementation of precoder 14 is illustrated in FIG. 2. The w_j information is input via terminal 30 to a first path having a plurality of exclusive OR gates 34, 36. The z_j information is input to a second path having a plurality of exclusive OR gates 40, 42, 44 via input terminal 32. A first feedback path is coupled to obtain the precoded data x_j from the first path, and includes a delay 38 (e.g., a flip-flop) for providing previous data x_{j-1} . A second feedback path is coupled to obtain the precoded data y_j from the second path. The second feedback path includes delay means 46 for providing previous data y_{j-1} . The first and second feedback paths have at least one common exclusive OR gate 48 and one common AND gate 50. Those skilled in the art will appreciate that the implementation illustrated in FIG. 2 will process the w_j and z_j information in accordance with the precoder relationships set forth above in order to provide the x_j and y_j terms which result in rotational invariance when combined with a transparent BCC and the rotationally invariant labeling of the signal set.

A preferred implementation of a postcoder 130 is illustrated in FIG. 3. The x_j' term is input via terminal 60 to a first path having a plurality of exclusive OR gates 64, 66 for providing the w_j' information. The y_j' information is input

via terminal 62 to a second path having a plurality of exclusive OR gates 70, 76 for providing the z_j' information. An AND gate 74 has a first input coupled to receive the exclusive OR of the precoded data x_j' and y_j' from the first and second paths, respectively, via exclusive OR gate 70. AND gate 74 has a second input coupled to receive the exclusive OR of delayed signals x_{j-1}' and y_{j-1}' from the first and second paths, respectively, via delays (e.g., flip-flops) 68, 78 and exclusive OR gate 72. The output of AND gate 74 is coupled to an input of exclusive OR gate 64 in the first path. The postcoder 130 illustrated in FIG. 3 will therefore process the x_j' and y_j' data recovered from the communication channel in accordance with the postcoder relationships set forth above.

FIG. 4 illustrates a rotationally invariant labeling in accordance with a QPSK implementation of the present invention. The numbers adjacent the symbol groups X, +, *, and o are octal references. The QPSK signal space 80 includes four points, each in one of the four symbol groups. The rotationally invariant labeling of the present invention is such that the least significant bits of symbol X are (0,0), of symbol + are (1,0), of symbol * are (1,1), and of symbol o are (0,1). Thus, it can be seen that under counterclockwise rotation by 90°, 180°, 270° and 360° the labels will change as follows:

$$(0,0)_X \rightarrow (1,0)_+ \rightarrow (1,1)_* \rightarrow (0,1)_o \rightarrow (0,0)_X.$$

If the two bits labeling the four points in the QPSK signal space 80 are denoted by (I_j, Q_j) , then it can be seen that the following relationship is satisfied:

$$(I_j, Q_j) \rightarrow (\bar{Q}_j, I_j) \rightarrow (\bar{I}_j, \bar{Q}_j) \rightarrow (Q_j, I_j) \rightarrow (I_j, Q_j).$$

To extend this labeling to QAM modulation, the points are labeled in such a way that (1) the two least significant bits, (I_j, Q_j) satisfy $(I_j, Q_j) \rightarrow (\bar{Q}_j, I_j)$ under 90° rotation and (2) the remaining most significant bits are invariant to 90° rotation. Such a labeling exists for all 90° symmetric QAM signal sets (e.g., square and cross constellations).

FIG. 5 illustrates such a labeling for a 16-QAM implementation. Again, the labeling of the symbols is indicated in octal, and complies with the labeling convention set forth above. In the 16-QAM implementation, the signal space 90 contains four modulation levels 91, 93, 95 and 97. Modulation level 93, for example, contains the four points + (labeled octal 06), * (labeled octal 07), o (labeled octal 05), and X (labeled octal 04). Octal 04 is represented in binary by the bits "0100". Octal 06 is represented by "0110". Octal 07 is "0111" and octal 05 is "0101". Any 90° counterclockwise rotation within modulation level 93 of signal space 90 will permute and complement the left one of the two least significant bits, with the two most significant bits remaining invariant. This can be seen by comparing signal point + (octal 06) to signal point * (octal 07), in which the least significant bits change from "10" to "11" complying with the relationship $(I_j, Q_j) \rightarrow (\bar{Q}_j, I_j)$. At the same time, the most significant bits "01" remain the same for each of the points + and * in modulation level 93. The labeling convention holds true for each and every point within the 16-QAM constellation illustrated in FIG. 5.

FIG. 6 illustrates a 64-QAM implementation. Again, the labeling convention holds for each and every point within signal space 94. As with FIGS. 4 and 5, each of the symbols in FIG. 6 is annotated with its octal representation.

The rotational invariance provided by the present invention can be easily understood by referring to the symbol labeling of FIGS. 4-6. For simplicity, it is helpful to refer to FIG. 5, where it can be seen that the counterclockwise progression from an X to a + will always represent a 90°

phase shift, regardless of where the actual points appear in the signal space. If the whole signal space is shifted by 90°, 180° or 270°, the relationship between the X symbol and + symbol will still be 90°. Similarly, an * symbol will always represent a 90° shift from a +, an o will always represent a 90° shift from an *, and an X will always represent a 90° shift from an o. Rotational invariance is achieved by encoding into the phase change, and not relying on the actual phase value.

FIG. 7 illustrates a decoder that can be used in accordance with the present invention. Data received from a transmission channel is input via terminal 100 to a conventional receiver and adaptive equalizer 102. Separate processing hardware 104, 106 is illustrated for each of the in-phase (I) and quadrature phase (Q) data, although much of the hardware could be shared in an integrated circuit implementation, as well known in the art.

The data represented as I data is pruned by a pruner 108 into uncoded bits which are delayed by a buffer (e.g., flip-flop) 110 before being input to a selector 118. The coded bits are input to a sequence estimator 112, which can comprise a standard Viterbi decoder. Algorithms other than the Viterbi algorithm, such as sequential decoding algorithms, could alternatively be used. The sequence estimator recovers the precoded bits s_j' (as precoded by precoder 14 at 25 the encoder), which are reencoded by a BCC encoder 114. The reencoded precoded bits provide control signals for actuating selector 118 to choose the appropriate uncoded bits u_j' for combination with the recovered and postcoded stream of coded bits w_j' and z_j' in a combiner 132.

Selector 118 can comprise, for example, a multiplexer arrangement in which the two bits from the BCC encoders 114, 126 are used to select among four possible combinations of the uncoded data bits output from delay stages 110, 122. The uncoded bits are the most significant bits of the symbol, and are rotationally invariant. Once the coded bits have been identified by the sequence estimators and reencoded by the BCC encoders 114, 126, they will identify, due to the mapping used, whether the I data path or Q data path MSBs are the proper ones to select. In an alternative implementation, selector 118 could be a lookup table that is addressed by the two bits output from the BCC encoders 114, 126.

The recovered coded bits for the data designated as I data are processed by an optional feedforward matrix 116 which is the inverse of the optional feedback matrix 18 shown in FIG. 1. These bits (X_j') are then postcoded in postcoder 130, which was discussed above in connection with FIG. 3.

The processing of the data designated Q data is identical to that designated I data. A pruner 120 prunes the uncoded bits, which are delayed by buffer 122 before being input to selector 118. Sequence estimator 124, BCC encoder 126, and optional feedforward matrix 128 are equivalent to elements 12, 114 and 116.

It should be noted in connection with the decoder of FIG. 7 that the decoded data will be the same regardless of any multiple of 90° rotation of the input data. The postcoder 130, the reencoders 114 and 126 and the optional feedforward matrices 116 and 128 have no feedback and thus error propagation is limited by providing, in effect, an output that is a sliding-window function of its input. In addition, error propagation of the decoded bits, as they pass through the uncoder, is typically dominated by the error propagation in the reencoder (114, 126).

FIG. 8 illustrates an example of a BCC encoder ($F(D)=1$) that can be used for the encoders 22, 24, 114 and 126 illustrated in FIGS. 1 and 7. Although any transparent BCC can be used in accordance with the invention, the following punctured rate $\frac{5}{6}$ and rate $\frac{3}{4}$ codes are provided as examples:

RATE 4/5

Punctured $\frac{5}{6}$, 16-state, $D_{pw} = 3$, $NN = 2$

$$G_0 = (1 + D^2 + D^4, 1 + D + D^2 + D^3 + D^4)$$

(Octal: 25,37)

$$P = \begin{pmatrix} 1000 \\ 1111 \end{pmatrix}$$

$$G = \begin{pmatrix} 1+D & 1+D & 1 & 1 & 1 \\ 0 & D & 1+D & 1 & 1 \\ D & D & D & 1+D & 1 \\ 0 & D & D & D & 1+D \end{pmatrix}$$

$$H = (1 + D + D^2 + D^3 + D^4, 1 + D^2 + D^4, D + D^3 + D^4, D + D^4, D + D^2 + D^4)$$

RATE 3/4

Punctured $\frac{3}{4}$, 16-state, $D_{pw} = 4$, $NN = 8$

$$G_0 = (1 + D^2 + D^4, 1 + D + D^2 + D^3 + D^4)$$

(Octal: 25,37)

$$P = \begin{pmatrix} 100 \\ 111 \end{pmatrix}$$

$$G = \begin{pmatrix} 1 & 1+D & 1+D & 1 \\ D & D & 1+D & 1+D \\ D^2 & D + D^2 & D & 1+D \end{pmatrix}$$

$$H = (1 + D + D^2 + D^3 + D^4, 1 + D^2 + D^4, D + D^3 + D^4, D + D^4, D + D^2 + D^4)$$

It should now be appreciated that the present invention provides rotationally invariant trellis codes for use with, e.g., QPSK and QAM transmission systems. The method of coding involves the use of a transparent binary convolutional code, a unique two-dimensional signal space mapping, together with a precoding and postcoding function which renders the postcoder output the same regardless of the phase of its input.

Although the invention has been described in connection with various preferred embodiments, it should be appreciated that numerous adaptations and modifications may be made thereto without departing from the spirit and scope of the invention as set forth in the claims.

I claim:

1. A rotationally invariant trellis coder for encoding input data to be transmitted to a receiver via a two-dimensional symbol modulation, comprising:
a precoder for processing said input data, said precoder comprising nonlinear logic that is the inverse of logic provided by a counterpart postcoder at said receiver;
an encoder for encoding the precoded data using a transparent binary convolutional code; and
means for mapping the encoded data from said encoder to a two-dimensional signal space having a plurality of signal points, said points being labeled with unique binary codes in which the two least significant bits, denoted by (I_j, Q_j) , are permuted and partially complemented to (\bar{Q}_j, \bar{I}_j) for each 90° phase rotation around the signal space in a counter clockwise direction, the remaining most significant bit for each point, if any, being invariant to such rotation.
2. A trellis coder in accordance with claim 1 wherein said precoder converts a first input data stream w_j and a second input data stream z_j to corresponding precoded data streams

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x_j and y_j , respectively, using feedback of delayed data x_{j-1} and y_{j-1} in accordance with the relationships:

$$x_j = w_j \oplus x_{j-1} \oplus z_j O(x_{j-1}, \Theta y_{j-1}),$$

and

$$y_j = z_j \oplus w_j \oplus y_{j-1} \oplus z_j O(x_{j-1}, \Theta y_{j-1}).$$

3. A trellis coder in accordance with claim 2 wherein the x_j and y_j data streams output from said precoder are convolutionally encoded to provide the two least significant bits of symbols that are mapped to the signal points in said signal space.

4. A trellis coder in accordance with claim 3 further comprising:

means for parsing uncoded bits from said input data for use by said mapping means;

wherein said uncoded bits represent the most significant bits of said symbols that are mapped to the signal points in said signal space.

5. A decoder for use in decoding symbols output from the trellis coder of claim 1, comprising:

at least one sequence estimator for use in recovering said precoded data from a received data stream;

wherein said postcoder receives and processes the recovered precoded data to provide output data that is invariant to 90° rotations of the recovered precoded data.

6. A decoder in accordance with claim 5 further comprising:

means for pruning said received data stream to recover coded and uncoded bits therefrom, said coded bits being input to said sequence estimator;

means for selecting uncoded in-phase (I) data or uncoded quadrature phase (Q) data for combination with the output data from said postcoder; and

means for reencoding the precoded data recovered by said sequence estimator for use in actuating said selecting means to select said uncoded I data or said uncoded Q data.

7. A decoder in accordance with claim 5 wherein:
said precoder converts a first input data stream w_j and a second input data stream z_j to corresponding precoded data streams x_j and y_j , respectively, using feedback of delayed data x_{j-1} and y_{j-1} in accordance with the relationships:

$$x_j = w_j \oplus x_{j-1} \oplus z_j O(x_{j-1}, \Theta y_{j-1}),$$

and

$$y_j = z_j \oplus w_j \oplus y_{j-1} \oplus z_j O(x_{j-1}, \Theta y_{j-1});$$

said postcoder converts the recovered precoded data comprising data streams x_j' and y_j' to first and second output data streams w_j' and z_j' , respectively, in accordance with the relationships:

$$w_j' = x_j' \oplus y_{j-1}' \oplus (x_j \oplus y_j) O(x_{j-1}, \Theta y_{j-1}),$$

and

$$z_j' = y_j' \oplus x_j' \oplus y_{j-1}' \oplus x_{j-1}'.$$

8. A decoder in accordance with claim 5, wherein said transparent binary convolutional code is a punctured code.

9. A precoder for use in a rotationally invariant trellis coder comprising:

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a first path having a plurality of exclusive OR gates for converting a first input data stream w_j to a corresponding precoded data stream x_j ;

a second path having a plurality of exclusive OR gates for converting a second input data stream z_j to a corresponding precoded data stream y_j ;

a first feedback path coupled to obtain said precoded data stream x_j from said first path, said first feedback path including delay means for providing previous data x_{j-1} ;

a second feedback path coupled to obtain said precoded data stream y_j from said second path, said second feedback path including delay means for providing previous data y_{j-1} ;

said first and second feedback paths having at least one common exclusive OR gate and at least one common AND gate; and

said precoder converting said first and second input data streams to said precoded data streams in accordance with the relationships:

$$x_j = w_j \oplus x_{j-1} \oplus z_j O(x_{j-1}, \Theta y_{j-1}),$$

and

$$y_j = z_j \oplus w_j \oplus y_{j-1} \oplus z_j O(x_{j-1}, \Theta y_{j-1}).$$

10. A postcoder for use in combination with the precoder of claim 9 comprising:

a third path having a plurality of exclusive OR gates for producing an output data stream w_j' from a received precoded data stream x_j' ;

a fourth path having a plurality of exclusive OR gates for producing an output data stream z_j' from a received precoded data stream y_j' ; and

an AND gate having a first input coupled to receive the exclusive OR of the precoded data streams x_j' and y_j' from said third and fourth paths, respectively, and a second input coupled to receive the exclusive OR of delayed data streams x_{j-1}' and y_{j-1}' from said third and fourth paths, respectively, said AND gate having an output coupled to an input of one of the exclusive OR gates in said third path;

said postcoder producing said output data streams w_j' and z_j' from said precoded data streams x_j' and y_j' in accordance with the relationships:

$$w_j' = x_j' \oplus y_{j-1}' \oplus (x_j \oplus y_j) O(x_{j-1}, \Theta y_{j-1}),$$

and

$$z_j' = y_j' \oplus x_j' \oplus y_{j-1}' \oplus x_{j-1}'.$$

11. A postcoder for use in a rotationally invariant trellis decoder comprising:

a first path having a plurality of exclusive OR gates for providing an output data stream w_j' from a received precoded data stream x_j' recovered using a sequence estimation algorithm;

a second path having a plurality of exclusive OR gates for providing an output data stream z_j' from a received precoded data stream y_j' recovered using said sequence estimation algorithm; and

an AND gate having a first input coupled to receive the exclusive OR of the precoded data streams x_j' and y_j' from said first and second paths, respectively, and a second input coupled to receive the exclusive OR of delayed data streams x_{j-1}' and y_{j-1}' from said first and

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second paths, respectively, said AND gate having an output coupled to an input of one of the exclusive OR gates in said first path; said postcoder producing said output data streams w_j' and z_j' from said precoded data streams x_j' and y_j' in accordance with the relationships:

$$w_j' = x_j \oplus y_{j-1} \oplus (x_j \oplus y_j) \odot (x_{j-1} \oplus y_{j-1}).$$

and

$$z_j' = y_j \oplus x_j \oplus y_{j-1} \oplus x_{j-1}'.$$

12. A method for coding digital data to enable rotationally invariant trellis coded modulation thereof, comprising the steps of:

precoding a stream of bits to be coded to render them rotationally invariant when encoded with a transparent binary convolutional code and subsequently decoded and postcoded at a receiver; encoding the precoded bits using said transparent binary convolutional code to provide coded information; and mapping the coded information to a two-dimensional signal space having a plurality of signal points, said points being labeled with unique binary codes in which the two least significant bits, denoted by (I_j, Q_j) , are permuted and partially complemented to (\bar{Q}_j, \bar{I}_j) for each 90° phase rotation around the signal space in a counter clockwise direction, the remaining most significant bits for each point, if any, being invariant to such rotation.

13. A method in accordance with claim 12 wherein said coded information is representative of in-phase (I) and quadrature phase (Q) data, said method comprising the further steps of:

transmitting the I and Q data over a communication channel in accordance with said signal space mapping; receiving and demodulating the I and Q data from said communication channel; decoding the coded information for the I and Q data to recover the precoded bits; and postcoding the recovered precoded bits to reverse the effect of said precoding step and recover said stream of bits.

14. A method in accordance with claim 12 comprising the further step of:

parsing said data prior to said precoding step into a stream of uncoded bits and said stream of bits to be coded; wherein said uncoded bits are mapped to the most significant bits of signal points in said signal space and the coded information derived from said stream of bits to be coded is mapped to the least significant bits of said signal points.

15. A method in accordance with claim 14 wherein said uncoded bits and coded information are representative of in-phase (I) and quadrature phase (Q) data, said method comprising the further steps of:

transmitting the I and Q data over a communication channel in accordance with said signal space mapping; receiving and demodulating the I and Q data from said communication channel;

pruning the demodulated I data to recover corresponding uncoded bits and coded information;

pruning the demodulated Q data to recover corresponding uncoded bits and coded information;

decoding the pruned coded information for the I and Q data to recover the precoded bits;

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postcoding the recovered precoded bits to recover the stream of bits that was coded;

reencoding the recovered precoded bits using said transparent binary convolutional code to provide control signals; and

selecting uncoded bits pruned from said I data or from said Q data in response to said control signals for combination with the stream of bits recovered by said postcoding step in order to reconstruct said digital data.

16. A rotationally invariant trellis coder for encoding input data to be transmitted to a receiver via a two-dimensional symbol modulation, comprising:

a precoder for processing said input data, said precoder comprising nonlinear logic that is the inverse of logic provided by a counterpart postcoder at said receiver; an encoder for encoding the precoded data using a transparent binary convolutional code; and

means for mapping the encoded data from said encoder to a two-dimensional signal space having a plurality of signal points, said points being labeled with unique binary codes in which the two least significant bits, denoted by (I_j, Q_j) , are permuted and partially complemented to (\bar{Q}_j, \bar{I}_j) for each 90° phase rotation around the signal space, the remaining most significant bits for each point, if any, being invariant to such rotation;

wherein said precoder converts a first input data stream w_j and a second input data stream z_j to corresponding precoded data streams x_j and y_j , respectively, using feedback of delayed data x_{j-1} and y_{j-1} in accordance with the relationships:

$$x_j = w_j \oplus x_{j-1} \oplus z_j \odot (x_{j-1} \oplus y_{j-1}).$$

and

$$y_j = z_j \oplus w_j \oplus y_{j-1} \oplus x_j \odot (x_{j-1} \oplus y_{j-1}).$$

17. A trellis coder in accordance with claim 16 wherein the x_j and y_j data streams output from said precoder are convolutionally encoded to provide the two least significant bits of symbols that are mapped to the signal points in said signal space.

18. An apparatus comprising a rotationally invariant trellis coder for encoding input data to be transmitted to a receiver via a two-dimensional symbol modulation, and a decoder for use in decoding symbols output from the trellis coder, said coder comprising:

a precoder for processing said input data, said precoder comprising nonlinear logic that is the inverse of logic provided by a counterpart postcoder at said receiver; an encoder for encoding the precoded data using a transparent binary convolutional code; and

means for mapping the encoded data from said encoder to a two-dimensional signal space having a plurality of signal points, said points being labeled with unique binary codes in which the two least significant bits, denoted by (I_j, Q_j) , are permuted and partially complemented to (\bar{Q}_j, \bar{I}_j) for each 90° phase rotation around the signal space, the remaining most significant bits for each point, if any, being invariant to such rotation;

said decoder comprising:

at least one sequence estimator for use in recovering said precoded data from a received data stream; wherein said postcoder receives and processes the recovered precoded data to provide output data that is invariant to 90° rotations of the recovered precoded data.

19. An apparatus in accordance with claim 18 wherein said precoder converts a first input data stream w_j and a second input data stream z_j to corresponding precoded data streams x_j and y_j , respectively, using feedback of delayed data x_{j-1} and y_{j-1} in accordance with the relationships:

$$x_j = w_j \oplus x_{j-1} \oplus z_j \odot (x_{j-1} \oplus y_{j-1}),$$

and

$$y_j = z_j \oplus w_j \oplus y_{j-1} \oplus z_j \odot (x_{j-1} \oplus y_{j-1}).$$

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20. An apparatus in accordance with claim 19 wherein the x_j and y_j data streams output from said precoder are convolutionally encoded to provide the two least significant bits of symbols that are mapped to the signal points in said signal space.

21. An apparatus in accordance with claim 18, said decoder further comprising:

means for pruning said received data stream to recover coded and uncoded bits therefrom, said coded bits being input to said sequence estimator;

means for selecting uncoded in-phase (I) data or uncoded quadrature phase (Q) data for combination with the output data from said postcoder; and

means for reencoding the precoded data recovered by said sequence estimator for use in actuating said selecting means to select said uncoded I data or said uncoded Q data.

22. An apparatus in accordance with claim 18 wherein: said precoder converts a first input data stream w_j and a second input data stream z_j to corresponding precoded data streams x_j and y_j , respectively, using feedback of delayed data x_{j-1} and y_{j-1} in accordance with the relationships:

$$x_j = w_j \oplus x_{j-1} \oplus z_j \odot (x_{j-1} \oplus y_{j-1}),$$

and

$$y_j = z_j \oplus w_j \oplus y_{j-1} \oplus z_j \odot (x_{j-1} \oplus y_{j-1});$$

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and

said postcoder converts the recovered precoded data comprising data streams x_j' and y_j' to first and second output data streams w_j' and z_j' , respectively, in accordance with the relationships:

$$w_j' = z_j \oplus y_{j-1} \oplus (x_j \oplus y_j) \odot (x_{j-1} \oplus y_{j-1}),$$

and

$$z_j' = y_j \oplus x_j \oplus y_{j-1} \oplus x_{j-1}'.$$

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23. A decoder in accordance with claim 18, wherein said transparent binary convolutional code is a punctured code.

24. A method for coding digital data to enable rotationally invariant trellis coded modulation thereof, comprising the steps of:

precoding a stream of bits to be coded to render them rotationally invariant when encoded with a transparent binary convolutional code and subsequently decoded and postcoded at a receiver;

encoding the precoded bits using said transparent binary convolutional code to provide coded information; and mapping the coded information to a two-dimensional signal space having a plurality of signal points, said

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points being labeled with unique binary codes in which the two least significant bits, denoted by (I_p, Q_p) , are permuted and partially complemented to (\bar{Q}_p, \bar{I}_p) for each 90° phase rotation around the signal space, the remaining most significant bits for each point, if any, being invariant to such rotation; wherein:

said precoding converts a first input data stream w_j and a second input data stream z_j to corresponding precoded data streams x_j and y_j , respectively, using feedback of delayed data x_{j-1} and y_{j-1} in accordance with the relationships:

$$x_j = w_j \oplus x_{j-1} \oplus z_j \odot (x_{j-1} \oplus y_{j-1}),$$

and

$$y_j = z_j \oplus w_j \oplus y_{j-1} \oplus z_j \odot (x_{j-1} \oplus y_{j-1}).$$

25. A method in accordance with claim 24 wherein said coded information is representative of in-phase (I) and quadrature phase (Q) data, said method comprising the further steps of:

transmitting the I and Q data over a communication channel in accordance with said signal space mapping; receiving and demodulating the I and Q data from said communication channel;

decoding the coded information for the I and Q data to recover the precoded bits; and

postcoding the recovered precoded bits to reverse the effect of said precoding step and recover said stream of bits.

26. A method in accordance with claim 24 comprising the further step of:

parsing said data prior to said precoding step into a stream of uncoded bits and said stream of bits to be coded; wherein said uncoded bits are mapped to the most significant bits of signal points in said signal space and the coded information derived from said stream of bits to be coded is mapped to the least significant bits of said signal points.

27. A method in accordance with claim 26 wherein said uncoded bits and coded information are representative of in-phase (I) and quadrature phase (Q) data, said method comprising the further steps of:

transmitting the I and Q data over a communication channel in accordance with said signal space mapping; receiving and demodulating the I and Q data from said communication channel;

pruning the demodulated I data to recover corresponding uncoded bits and coded information;

pruning the demodulated Q data to recover corresponding uncoded bits and coded information;

decoding the pruned coded information for the I and Q data to recover the precoded bits;

postcoding the recovered precoded bits to recover the stream of bits that was coded;

reencoding the recovered precoded bits using said transparent binary convolutional code to provide control signals; and

selecting uncoded bits pruned from said I data or from said Q data in response to said control signals for combination with the stream of bits recovered by said postcoding step in order to reconstruct said digital data.

* * * * *

EXHIBIT C



United States Patent [19]

Heegard et al.

[11] Patent Number: 5,703,887

[45] Date of Patent: Dec. 30, 1997

[54] SYNCHRONIZATION AND ERROR DETECTION IN A PACKETIZED DATA STREAM

[75] Inventors: Chris Heegard, Ithaca, N.Y.; Andrew J. King, Phoenix, Ariz.; Sydney Lovel, Phoenix, Ariz.; Thomas J. Kokze, Phoenix, Ariz.

[73] Assignee: General Instrument Corporation of Delaware, Chicago, Ill.

[21] Appl. No.: 363,252

[22] Filed: Dec. 23, 1994

[51] Int. Cl. 6 H03M 13/00; H04L 7/00

[52] U.S. Cl. 371/42

[58] Field of Search 371/37.1, 42, 47.1

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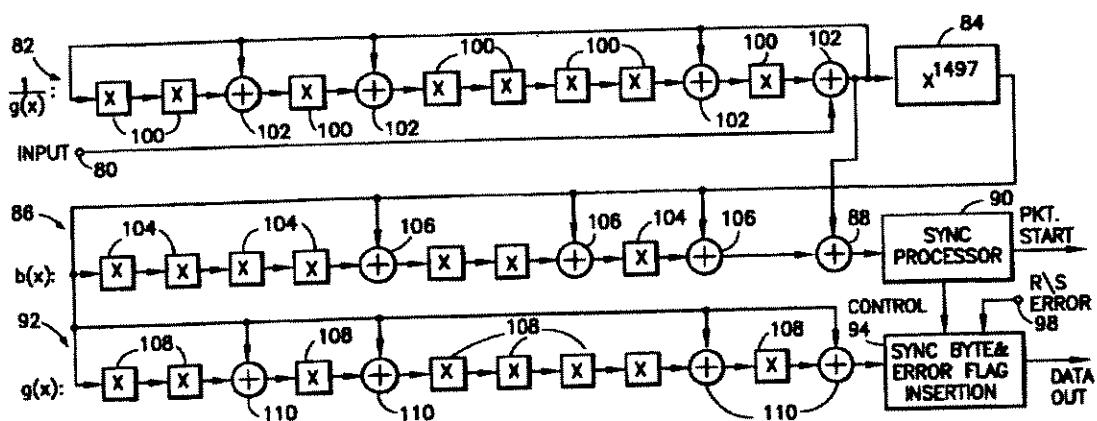
Primary Examiner—Stephen M. Baker

Attorney, Agent, or Firm—Barry R. Lipsitz; Ralph F. Hoppin

[57] ABSTRACT

A method and apparatus are provided for achieving synchronization and detecting errors in a data stream such as an MPEG-2 transport packet stream. In an MPEG embodiment, the MPEG sync word is removed and replaced with a parity code that is used at the decoder for both synchronization and error detection. A syndrome calculator in the decoder can be implemented using a unique one bit in, one bit out FIR filter. Codewords used to generate the parity code can be provided by a linear block code that is a dual of a shortened cyclic code.

24 Claims, 7 Drawing Sheets



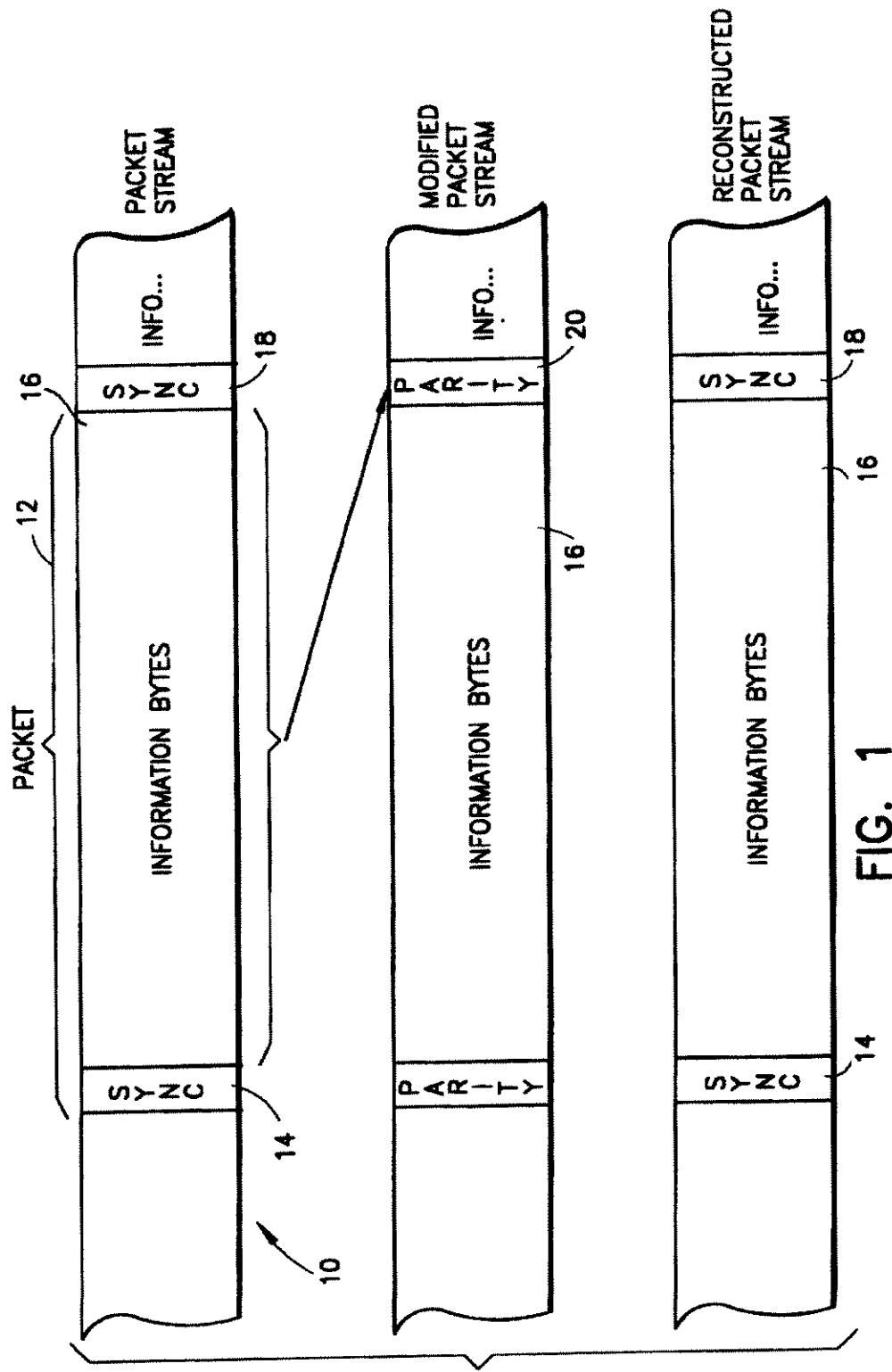


FIG. 1

FIG. 2

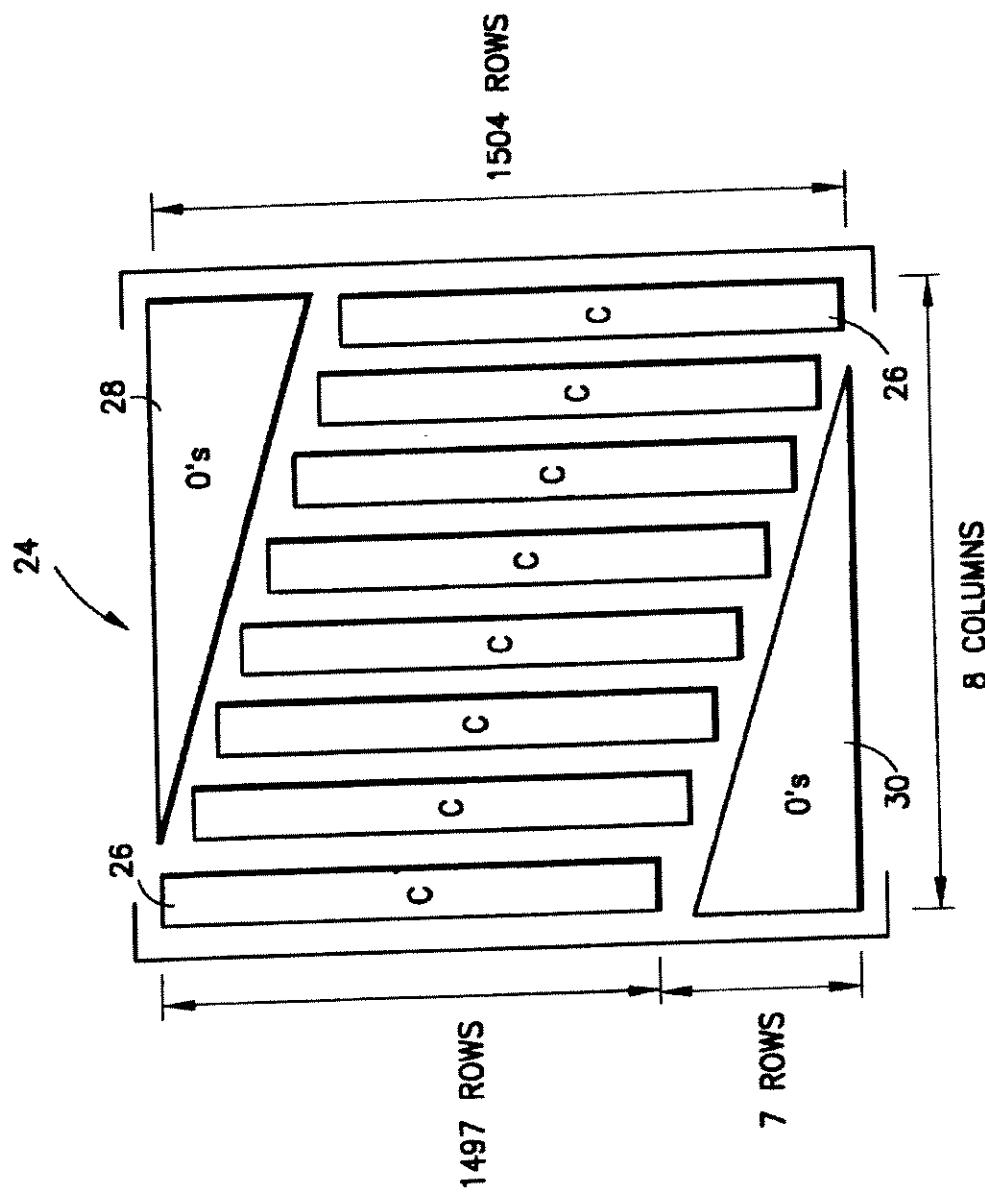
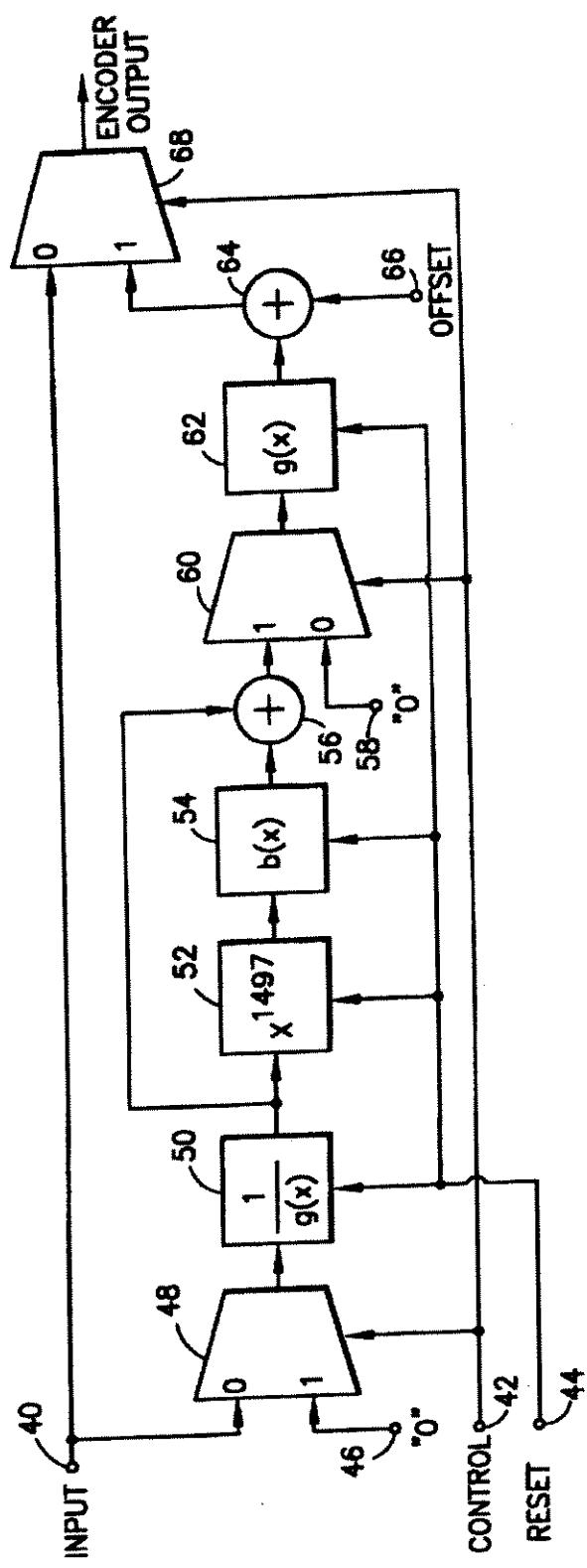


FIG. 3



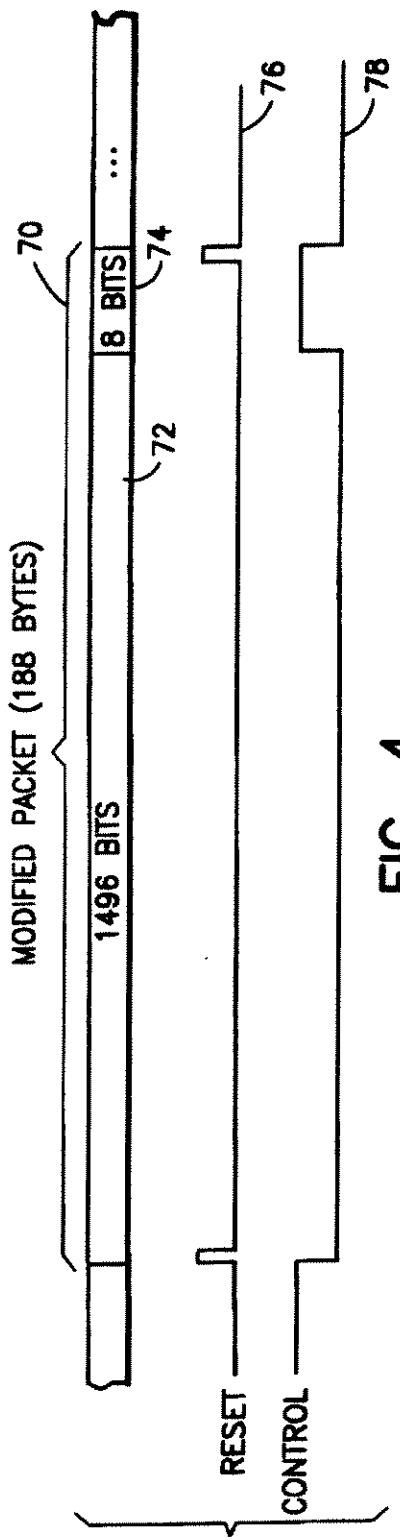


FIG. 4.

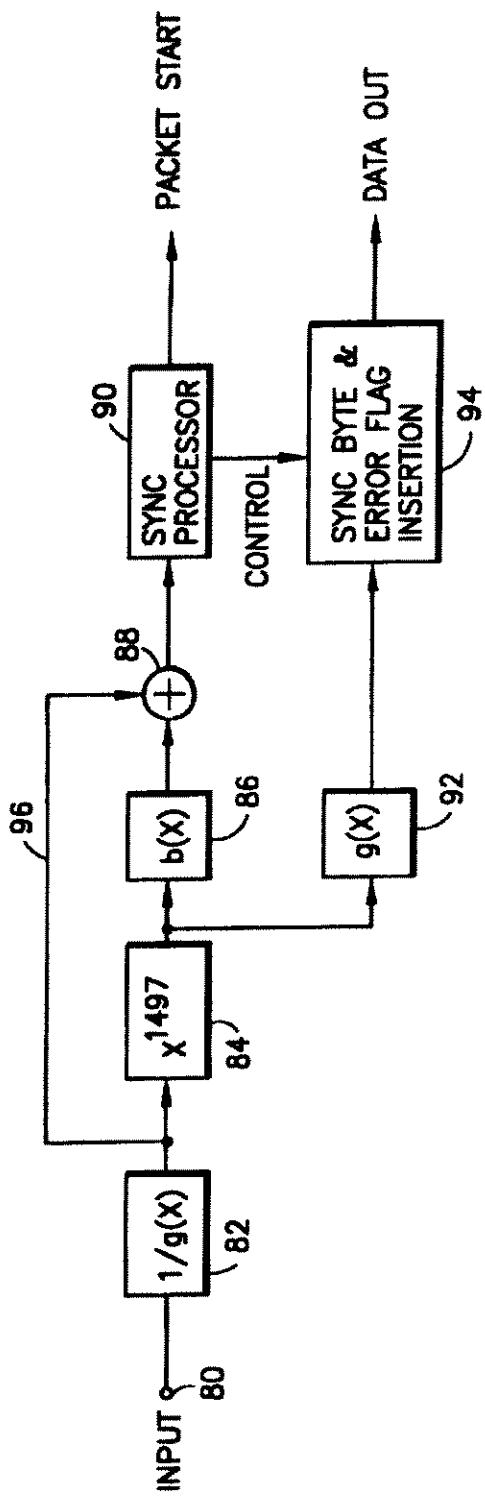


FIG. 5.

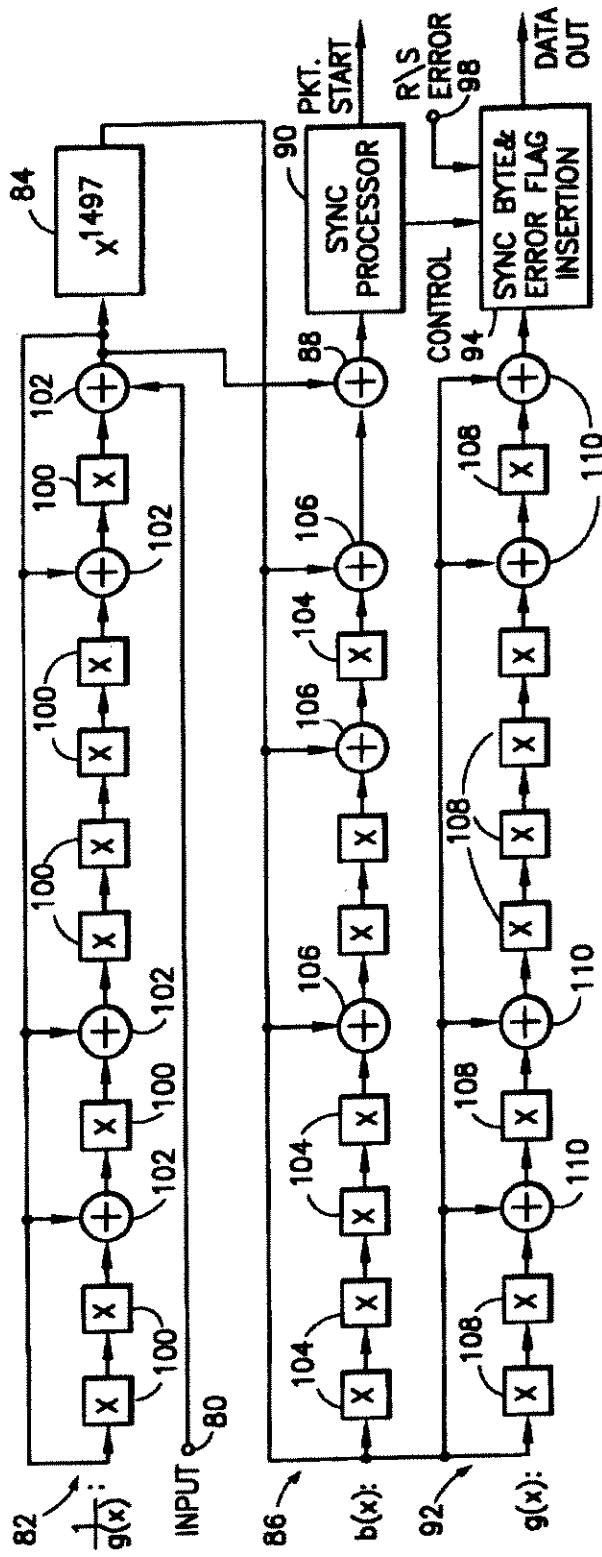


FIG. 6

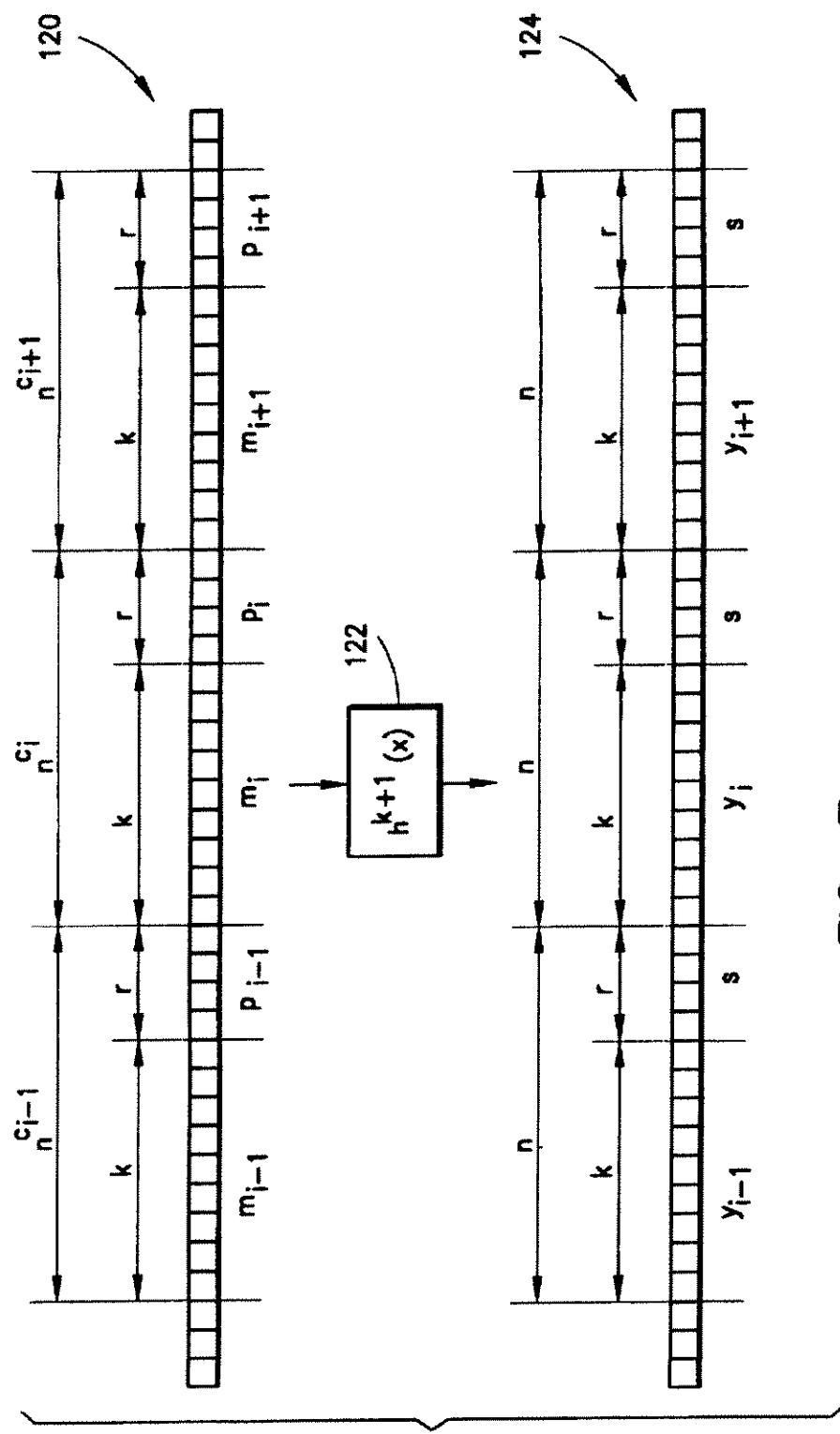


FIG. 7

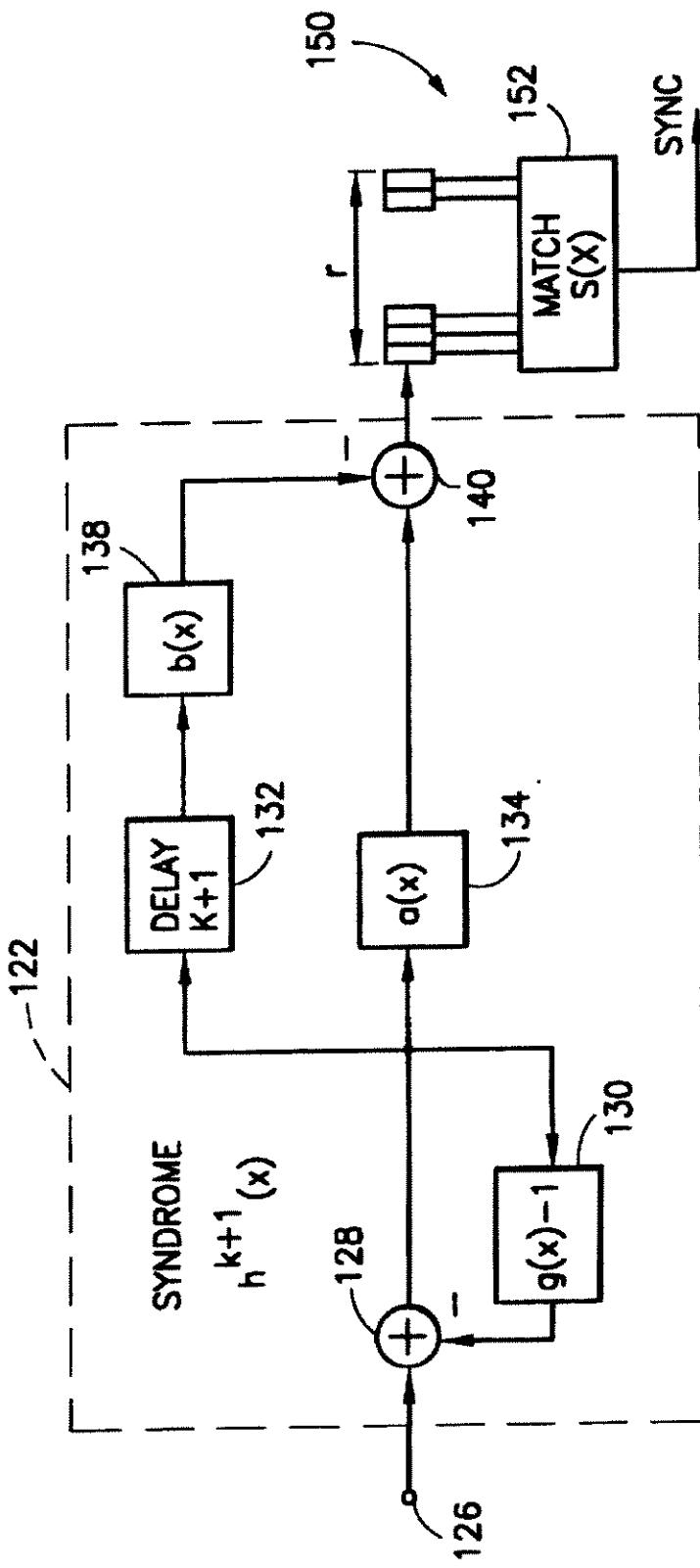


FIG. 8

SYNCHRONIZATION AND ERROR DETECTION IN A PACKETIZED DATA STREAM

BACKGROUND OF THE INVENTION

The present invention relates to a method and apparatus for achieving synchronization and detecting errors in a data stream, and more particularly to a method and apparatus for synchronization and error detection of an MPEG encoded data stream or the like.

The Motion Picture Experts Group (MPEG) has proposed a standard for the transport of digital data. The MPEG-2 standard is widely known and recognized as a video and audio compression specification, and has been sanctioned by the International Standards Organization (ISO) in document ISO 13818. The MPEG-2 specification also contains a systems "layer" that provides a transmission medium independent coding technique to build bitstreams containing one or more MPEG programs. The MPEG coding technique uses a formal grammar ("syntax") and a set of semantic rules for the construction of bitstreams to be transmitted. The syntax and semantic rules include provisions for multiplexing, clock recovery, synchronization, and error resiliency.

The MPEG transport stream is specifically designed for transmission in conditions that can generate data errors. MPEG transport packets each have a fixed length of 188 bytes. Many programs, each with different components, may be combined in a transport stream. Examples of services that can be provided using the MPEG format are television services broadcast over terrestrial, cable television or satellite networks as well as interactive telephony-based services. The primary mode of data transmission in MPEG broadcast applications will be the MPEG-2 transport stream. The syntax and semantics of the MPEG-2 transport stream are defined in the MPEG-2 Systems Committee draft, ISO/IEC JTC1/SC29/WG11/N0601, November 1993.

Multiplexing according to the MPEG-2 standard is accomplished by packaging raw elementary streams such as coded video and audio into packetized elementary stream (PES) packets which are then inserted into transport packets. As noted above, each transport packet is fixed at 188 bytes in length. The first byte is a synchronization byte having a unique eight-bit pattern, e.g., 01000111. The sync byte is used to locate the beginning of each transport packet.

The sync byte is followed by a three-byte prefix containing a transport packet error indicator, payload unit start indicator, transport priority bit, packet identifier (PID), transport scrambling control, adaptation field control and a continuity counter. Use of the sync byte and three prefix bytes leave up to 184 bytes in the transport packet for the actual data to be communicated, referred to as the "payload." An optional adaptation field may follow the prefix, to carry both MPEG related and private information of relevance to a given transport stream or the elementary stream carried within a given transport packet. Whenever an adaptation field is present, the number of bytes in the payload will be reduced by the number of bytes used by the adaptation field. Further details of the MPEG-2 transport specification can be found in A. J. Wasilewski, "MPEG-2 Systems Specification: Blueprint for Network Interoperability," *Communications Technology*, February, 1994, pp. 30-44.

In the MPEG standard, the synchronization byte at the beginning of each transport packet is used merely to acquire synchronization at the decoder. The decoder searches a received serial bitstream formed from successive transport packets to locate a match with the unique synchronization

byte. The MPEG synchronization byte (01000111) was chosen due to its excellent aperiodic autocorrelation properties and because it is not easily emulated by PID values from the low end of the range. Upon finding a first synchronization byte, a typical decoder will initially assume it is a valid synchronization byte and subsequently determine if another such byte is received after the next 187 bytes of the serial bitstream have passed. After two or more successive synchronization bytes are located where expected, it is assumed that synchronization has been achieved, and that the data between the synchronization bytes comprises the prefix, adaptation field (if present) and payload of a transport packet. The payload data is processed in a conventional manner to recover the transmitted information.

It would be advantageous to provide a method and apparatus for utilizing the information bearing capacity of a synchronization byte in a transport stream such as an MPEG-2 transport stream. More particularly, it would be advantageous to provide an error detection capability in addition to the packet alignment information supplied by the synchronization byte. It would be still further advantageous to provide a simplified decoder for processing error detection information provided by the sync byte in order to identify those transport packets containing errors.

The present invention provides a method and apparatus having the aforementioned advantages in which parity checksums are used instead of sync bytes in successive transport packets. Linear block codes (LBCs) are generated for which the parity check equations can be implemented in a single finite impulse response (FIR) filter. By implementing the parity check equations in a single FIR filter, the cost and complexity of the decoder used for synchronization and error detection can be greatly reduced.

SUMMARY OF THE INVENTION

In accordance with the present invention, a method is provided for achieving synchronization and detecting errors in a data stream carrying successive packets of k information bits and r synchronization bits. The synchronization bits of each packet comprise a predefined, searchable pattern. At least one synchronization pattern is located in the data stream to enable the boundaries for the k information bits of successive packets to be determined. In one embodiment, the synchronization pattern in each packet is replaced with an r -bit parity code derived from a counterpart set of k information bits in the data stream, thereby generating a modified data stream. The modified data stream is communicated to a decoder. At least one of the parity codes is located in the modified data stream at the decoder to achieve synchronization. This enables the boundaries for the k information bits of successive packets to be determined. Once synchronization has been achieved, the parity codes are compared to checksums obtained from their counterpart k information bits at the decoder to determine when the information bits in a received packet contain an error.

The data stream can comprise an MPEG compatible data stream, e.g., an MPEG-2 data stream or a similarly formatted data stream. The parity codes can be scaled such that when decoded at the decoder, they will match MPEG synchronization patterns. In an MPEG-2 embodiment, the number of information bits (prefix, adaptation field and payload) in a packet is $k=1496$. In a preferred MPEG implementation, the synchronization pattern for each packet precedes the k information bits of that packet, whereas the counterpart set of k information bits for each parity code comprises the k information bits immediately preceding the

parity code. The parity code can be generated from a linear block code comprising a dual of a shortened cyclic code.

Communication apparatus in accordance with the present invention enables a receiver to robustly obtain synchronization and detect errors in a data stream carrying successive packets of k information bits and an r -bit parity code. The parity code of each packet comprises a predefined pattern of bits detectable at the receiver by searching for the pattern. The parity code also functions as a checksum for information bits carried in the data stream. The apparatus comprises means for inserting the parity codes in the packets prior to communication to the receiver. Each of the parity codes is derived from a counterpart set of k information bits in the data stream. Means are provided for communicating the data stream to the receiver after insertion of the parity codes. At least one parity code is located in the data stream at the receiver to achieve synchronization. This enables the boundaries for the k information bits of successive packets to be determined. In accordance with the invention, the receiver also includes means for comparing the parity codes to checksums obtained from their counterpart k information bits to determine when the information bits in a packet contain an error.

The data stream into which the parity codes are inserted can comprise, for example, an MPEG compatible data stream in which successive transport packets each commence with a synchronization pattern followed by the k information bits. In such an instance, the apparatus can further comprise means for replacing the synchronization patterns with the parity codes to provide a modified data stream for communication to the receiver. In an illustrated embodiment, each parity code that is substituted for the synchronization pattern is derived from the k information bits of the preceding packet. Thus, whereas the synchronization pattern for each transport packet is at the beginning of the packet and is followed by the k information bits carried by that packet, the parity code that is substituted for the synchronization pattern is derived from the previous k information bits, which are carried by the preceding packet.

The parity codes can be scaled at the encoder so that when decoded at the receiver, they will match an MPEG synchronization pattern. The receiver can further comprise means for reconstructing the data stream from the modified data stream by replacing the parity codes with the synchronization patterns, after the parity codes have been used to obtain synchronization and detect errors. In the illustrated embodiment, a parity check matrix is provided at the receiver for generating a predefined synchronization pattern from valid parity codes. The predefined synchronization pattern can comprise, for example, a standard MPEG synchronization pattern.

The present invention also provides a decoder for a packetized digital data stream. The data stream contains successive packets, each having k information bits and an r -bit parity code. The parity code of each packet is derived from k bits of information carried by the data stream. The decoder includes means for searching the data stream during a signal acquisition phase to locate a parity code contained therein. Means are provided for establishing a synchronization condition based on one or more parity codes located by the searching means. A checksum derived from the k information bits of each packet is compared to the parity code for those k information bits during a tracking phase. Means are provided for signaling an error in the k information bits for a packet when the checksum for those bits does not match the parity code therefor.

The decoder can further comprise means for monitoring the parity codes during the tracking phase. Means responsi-

sive to the monitoring means are provided for switching from the tracking phase to the acquisition phase after a predetermined plurality of r -bit patterns considered by the monitoring means to be parity codes are found to be invalid.

Where the data stream is encoded in an MPEG compatible format, the decoder can further comprise means for replacing the parity code in each packet with an MPEG synchronization pattern after the parity code has served its purpose for acquisition and error detection. The parity code can be derived from the k information bits of the immediately preceding packet, whereas each synchronization pattern comprises the first r bits in a packet and is followed by the k information bits for that packet. In an illustrated embodiment, the parity codes are generated from a linear block code comprising a dual of a shortened cyclic code.

The invention also provides apparatus for calculating syndromes for linear block coded codewords. The apparatus comprises a finite impulse response filter having an input for receiving a serial bitstream of codeword data, each codeword containing k information bits and r parity bits, said filter having an output for providing a serial bitstream of syndromes. The syndromes comprise a fixed linear combination of a current bit of said codeword data input to said filter and the k previous bits of said codeword data. The filter has an impulse response $h^{k+1}(x)$, where:

$$h^{k+1}(x) = \frac{a(x) - x^{k+1}b(x)}{g(x)},$$

$g(x)$ is a generator polynomial of degree r describing a recursion, and

$a(x)$ and $b(x)$ are polynomials chosen such that the polynomial $h^{k+1}(x)$ will be of degree k , have a non-zero constant term $h_0=1$, and have a non-zero final term $h_k=1$.

The linear block code used to generate the codewords for which the syndromes are calculated can comprise a dual of a shortened cyclic code. Means can be provided at the output of the filter for detecting a synchronization pattern in the serial bitstream of syndromes.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagrammatic illustration of a packet stream, modified packet stream and reconstructed packet stream in accordance with the present invention;

FIG. 2 is a diagrammatic illustration of a parity check matrix in accordance with the present invention;

FIG. 3 is a block diagram of an encoder in accordance with the present invention;

FIG. 4 is a timing diagram illustrating the reset and control signals used in the encoder of FIG. 3;

FIG. 5 is a block diagram of a decoder in accordance with the present invention;

FIG. 6 is a block diagram illustrating the decoder of FIG. 5 in greater detail;

FIG. 7 is a diagrammatic illustration showing the function of the syndrome calculator in accordance with the present invention; and

FIG. 8 is a block diagram illustrating a one bit in, one bit out finite impulse response (FIR) filter used as a syndrome calculator with a shift register used for signal acquisition and synchronization purposes coupled to the output thereof.

DETAILED DESCRIPTION OF THE INVENTION

The present invention will be described herein primarily in connection with the communication of data in accordance

with the MPEG-2 transport syntax. However, it should be appreciated that the references to the MPEG-2 standard are for purposes of illustration only, and that the invention is also applicable to other transport schemes in which the transport packets include synchronization bits and information bits.

An MPEG encoded data stream consists of a continuous stream of packets each containing 188 bytes. The data stream is transmitted in serial fashion, most significant bit (MSB) first. The first byte of a packet is specified to be a sync word having a value 01000111 (0x47 in hexadecimal notation). The sync word is intended for use by a decoder to achieve alignment to packet boundaries.

The present invention incorporates an additional layer of processing to utilize the information bearing capacity of the sync word. In addition to the packet alignment information supplied by this word, additional error detection capability is realized in accordance with the present invention by replacing the sync word with a parity checksum. The processing necessary to accomplish this is performed at the transcoder and constitutes the outer most layer of encoding.

In the illustrated MPEG embodiment, the parity checksum is computed over the adjacent 187 bytes which constitute the information bits (as distinguished from the sync bits) of the immediately preceding MPEG packet. By replacing the sync word in one MPEG packet with a parity checksum for the information bits of the preceding MPEG packet, it is possible to simultaneously obtain packet synchronization and error detection of the information in the preceding packet. The decoder computes a sliding checksum on the serial data stream, using the detection of a valid codeword in place of a correlator function to detect the start of a packet. Once a locked alignment condition is established, the absence of a valid codeword at the expected location will indicate an errored packet condition. The error flag of the packet can then be set to indicate an errored data condition to the data processor. As the data is passed out of the decoder, the normal sync word can be reinserted in place of the checksum to provide a standard MPEG data stream.

the sync byte 18 of the next packet in the stream. This enables the parity code 20 to verify the integrity of the preceding information bytes 16 as well as to obtain packet synchronization.

After the modified packet stream has been acquired and error detection has been completed at the decoder, the original packet stream can be reconstructed as illustrated at the bottom of FIG. 1. In order to do this, the parity codes are replaced with the original synchronization bytes (e.g., the MPEG sync word 01000111) so that the packet stream will appear in its original form to subsequent decoder processes.

FIG. 2 illustrates a parity check matrix P generally designated 24 which can be used by the decoder to identify a valid codeword. The code is designed such that when a valid codeword is multiplied against the parity check matrix, a positive match is indicated when the calculated product produces a 0x47 (hexadecimal) result. This enables the utilization of conventional MPEG hardware to identify and synchronize to the standard MPEG sync word. The parity check calculation constitutes a preprocessing step which immediately precedes the conventional hardware.

The parity check matrix 24 is arranged such that it contains eight identical column structures 26. The replicated column structure (designated C) contains 1,497 bits of data for an MPEG embodiment. Proceeding from the left-most column in FIG. 2, the 1497-bit column C is duplicated in subsequent columns of the matrix, shifted down by one bit position in a circular fashion. In this way, the bit positions unoccupied by the column data are filled with zeros, as designated by reference numeral 28 at the top of the matrix and reference numeral 30 at the bottom thereof. An example of the contents of the 1497-bit columns 26 that can be used to form the parity check matrix 24 is illustrated in Table 1. All entries in the table are in hexadecimal format, except for the last entry which is a single binary one. The upper left entry in the table represents the top bit of the column C, and the lower right entry represents the bottom bit of the column.

TABLE 1

C =	b03	857f	97a5	0dd6	ebe0	cac3	58c1	2da9	a7ee	67b2
1099	2627	5688	a47c	05c7	78b3	61e7	0aff	2f4a	1bb7	
d741	9546	b182	5b33	4fd6	cfc4	2072	4c4e	ad11	48f8	
0b6e	f166	c3ce	15fe	5e94	3764	ae83	2a8d	6304	b6a6	
9fb9	9ec8	40e4	989d	5a22	91d0	171d	e2cd	879c	2bfc	
bd28	6edf	5d06	551a	c609	6d4d	3773	3d90	81c9	313a	
b445	23e0	2a3b	c39b	0f38	5789	7a50	dd1e	ba0c	aa35	
8c12	da96	7a66	7b21	0392	6275	688a	47c0	3c77	8b36	
1e70	aef2	94a1	bb7d	7419	546b	1825	b534	81cc	5f42	
0724	c4ea	d114	8f	a'b1]						

FIG. 1 illustrates the modification of a transport packet stream in accordance with the present invention. A packet stream 10, such as an MPEG packet stream, is formed from successive packets 12 each having r sync bits 14 followed by k information bits 16. In the MPEG format, the sync bits 14 comprise an eight-bit byte (r=8) followed by 187 eight-bit information bytes 16 (k=1496).

In order to enable both synchronization and error detection in accordance with the present invention, the sync bits 18 from a following packet are replaced with parity bits 20 to form a modified packet stream. The parity code 20 is an r bit checksum derived from the information bytes 16 of the preceding packet 12. Thus, whereas packet 12 comprises sync byte 14 followed by information bytes 16, the parity code 20 in the modified packet stream is in the position of

In interpreting the matrix, let:

R = received MPEG-2 packet, with 187 bytes followed
by the checksum byte, for a total of 1504 bits
S = row vector of length 1504 bits
= [first bit of packet, . . . most recent received bit].

Then,

S = PR, where

S = row vector of length 8 bits.

A valid received codeword is indicated when
S = [0100 0111] = 0 × 47.

By examination of the parity check matrix 24, and column C set forth in Table 1, it can be seen that each bit of the computed checksum can be derived from an FIR structure, consisting of 1497 taps. The same FIR structure can be used to compute all eight parity bits since each column of the

parity check matrix is offset by one bit position, but otherwise identical. The decoder implementation can therefore consist of a single 1497 tap FIR, computing each parity bit in a serial fashion. This result is computed over a binary field, and consequently all additions represent exclusive-OR operations and each tap coefficient is either a one or a zero.

Such an FIR implementation of the decoder is desirable so that errors introduced by either the communication channel or any soft upset mechanism do not propagate indefinitely. This structure will guarantee that error conditions flush out within the space of a packet.

FIG. 3 is a block diagram illustrating an encoder useful in accordance with the present invention. When the invention is used in connection with, e.g., digital cable television services, the encoder will be implemented in a transcoder at the cable television headend. The data stream to be encoded (1504 bits per packet in an MPEG implementation) is input via terminal 40. A modified packet structure 70 produced by the encoder of FIG. 3 is illustrated in FIG. 4. The modified packet (in an MPEG implementation) comprises 188 bytes of data. Of these, portion 72 comprises 1496 bits of information data (187 bytes) and portion 74 comprises the eight bits of parity data inserted by the encoder of FIG. 3. A reset signal 76 is input to the encoder via terminal 44. A control signal 78 is input to the encoder via terminal 42. In response to the control signal, the information bits 72 will be output from the encoder via selector 68 without modification. The encoder computes the parity bits 74 and inserts them into the modified packet in response to the control signal 78 going high. At this point, selector 68 will output the parity bits from exclusive-OR gate 64 instead of the synchronization byte carried in the original packet input via terminal 40. Selector 68 is actuated by the control signal to provide the input data packet to the FIR filter, which is implemented using components 50, 52, 54 and 62. Each of these components is reset at the packet boundaries by the reset signal input via terminal 44.

The encoder of FIG. 3 implements a systematic linear block code (LBC), in which the information bits 72 of the packet are processed to produce an eight-bit checksum. The checksum 74 is appended to the end of the information bits 72, as illustrated in FIG. 4.

The core function, including $1/g(x)$, the delay buffer 52 and the polynomial function $b(x)$ of the encoder is identical to the FIR function implemented in the decoder, discussed below in connection with FIGS. 5-8. Since packet alignment is already known, the delay buffer 52 can be replaced by a shift register which stores the first seven bits of a 187-byte data word. After 1497 bits have been passed through the core function 50, these seven bits can then be shifted into the polynomial function 54, providing a correct output which is then summed with the bits shifted out of block 50. These combined bits are then passed through box 62, which implements the polynomial function $g(x)$ to form an eight-bit result.

The eight-bit result out of block 62 can be scaled by an offset value input via terminal 66 to an exclusive-OR gate 64. If the offset value is set to 0x67 (hexadecimal), which exclusively ORs each respective bit output from block 62, a 0x47 (hexadecimal) result will be produced by the decoder when a valid codeword is detected. This result is the same as the MPEG codeword (01000111) which simplifies the decoder hardware by enabling the use of MPEG compatible components. If no offset were added by the encoder, then the decoder would be required to detect eight successive zeros, which has relatively poor autocorrelation characteristics and would increase the mean time required to achieve synchro-

nization. The final computed eight-bit result output from exclusive-OR gate 64 represents the checksum and is appended to the end of the 187-byte (1496 bit) information word 72 via selector 68.

FIG. 5 is a block diagram of an efficient structure that can be utilized to decode the data stream output by the encoder of FIG. 3. The decoder structure provided by the present invention results in a drastic reduction in hardware requirements over a conventional FIR structure. This is accomplished with an eight-tap infinite impulse response (IIR) feedback shift register (which generates a pseudo random sequence of maximal length), concatenated with an eight-tap FIR structure. The combined structure is implemented to realize a response equivalent to a 1497-tap FIR filter. The hardware implementation still requires the use of a 1497-bit delay buffer, but this is still much more economical to implement (e.g., with a random access memory based structure) compared to any shift register based approach. Power consumption is also greatly reduced since only a small number of circuit nodes will toggle over any clock period.

The decoder input bitstream is applied to the IIR filter 82 via input terminal 80. The function provided by the IIR filter is described as $1/g(x)$. The output bits are subsequently processed by an FIR function containing a single tap at the input to a 1497-bit buffer 84. At the output of the buffer 84, an additional eight taps are described by the function $b(x)$, illustrated as block 86. The output of this composite filter produces the desired 1497 tap FIR response and is input via exclusive-OR 88 to a sync processor 90, which attempts to identify the sync word. The output of the IIR filter is fed forward via line 96 as the other input to exclusive-OR 88. Upon identifying the sync word, sync processor 90 will output a packet start signal designating the commencement of successive packets in the input bitstream.

During acquisition, sync processor 90 functions in a mode that is similar to a standard MPEG sync detector. A shift register is used to store the most recent eight bits output from the filter structure, and these bits are examined for an occurrence of the 0x47 (hexadecimal) sync word. Once packet alignment has been established by the acquisition state machine, sync processor 90 will continue to attempt to locate the sync word at the expected time. If the sync word is absent, an error flag bit will be set in the delayed packet data stream. If any input bit originated from an errored block as identified by an error correcting code, e.g., a Reed-Solomon (R/S) code, an error latch will be set that causes the decoder to set the error flag of any packets that are output containing errored bits. This error latch will reset itself at the start of the next packet boundary. Reed-Solomon and other error detection codes and their implementation are well known in the art.

If the error flag of the current packet was previously set by the transcoder due to any errors, such as satellite transmission errors, the contents of the error flag will remain high at the output of the decoder.

The decoder input bitstream is reconstructed at the output of the delay buffer 84 by processing the delayed data by the generator polynomial $g(x)$ as indicated at box 92. This is the inverse of the IIR filter function $1/g(x)$. The data must be taken from the output of the packet delay buffer, so that detected data errors can be used to set the error flag corresponding to the packet in which they occurred.

As noted above, in an MPEG implementation it is advantageous to replace the parity code 74 inserted at the encoder with the standard MPEG synchronization byte once the parity code has achieved its purpose of acquiring synchro-

nization and detecting errors. The sync byte is reinserted, together with any necessary error flags, in the recovered data stream by sync byte and error flag insertion circuit 94. This circuit is responsive to a control signal from sync processor 90 which identifies the packet boundary at which the sync byte is to be reinserted. The reconstructed packet stream is output from circuit 94 ("data out").

FIG. 6 is a more detailed block diagram of the decoder filter shift registers. The IIR filter 82 comprises a sequence of one-bit delays (x) 100 and exclusive-OR gates 102. The polynomial function $b(x)$ provided by box 86 is implemented using a plurality of one-bit delays 104 and exclusive-OR gates 106. Similarly, the generator polynomial $g(x)$ provided by block 92 is implemented using one-bit delays 108 and exclusive-OR gates 110. The remaining components illustrated in FIG. 6 are the counterparts of the same components illustrated in FIG. 5. FIG. 6 also illustrates a terminal 48 for inputting the supplemental (e.g., R/S) error information to the sync byte and error flag insertion circuit 94.

FIGS. 7 and 8 are useful in describing the theory behind the decoder of the present invention, and more particularly the simplified FIR filter design used at the decoder for calculating syndromes (i.e., the parity bits) from the transport packets. In the following discussion, each transport packet is considered to be a linear block coded codeword C_r .

A binary linear block code (LBC) $C \subset F_2^n$ with parameters (n, k) consists of a k dimensional subspace of the set of binary n -tuples F_2^n . Such a space can be described by a set of k basis vectors placed in a $k \times n$ generator matrix

$$G = \begin{pmatrix} g_{1,1} & g_{1,2} & \dots & g_{1,n} \\ g_{2,1} & g_{2,2} & \dots & g_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ \vdots & \vdots & \ddots & \vdots \\ g_{k,1} & g_{k,2} & \dots & g_{k,n} \end{pmatrix}$$

Given a generator matrix, a (linear) encoder can be constructed via matrix multiplication

enc_G

where $\text{enc}_G \in F_2^{k \times n}$ is a binary k -tuple. If the first k columns of G is the identity matrix, we say that G represents a systematic encoder. Note that a given LBC C has many generator matrices (and encoders).

An alternate description of a code C is given by a set of $r=n-k$ linearly independent parity-check equations that can be expressed in terms of a parity-check matrix H , a $r \times n$ binary matrix. A binary vector of length n is a codeword if and only if

$$(c_0, c_1, \dots, c_{n-1}) \begin{pmatrix} h_{1,1} & h_{1,2} & \dots & h_{1,n} \\ h_{2,1} & h_{2,2} & \dots & h_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ \vdots & \vdots & \ddots & \vdots \\ h_{r,1} & h_{r,2} & \dots & h_{r,n} \end{pmatrix} = (0, 0, \dots, 0)$$

or
 $ch^T = 0$.

Again, a given LBC C has many parity-check matrices.

The space spanned by the rows of a given parity-check matrix H for a code C form an (n, r) LBC called the dual code. This code is described by

$$C^\perp = \{d \in F_2^n | d \cdot c = 0 \text{ for all } c \in C\}.$$

A coset of a LBC is obtained via solutions to the equation

$$ch^T = S$$

where S is a fixed binary vector of length r .

To encode onto a coset of a LBC, a constant vector can be added

$$c = G \cdot \sigma$$

where $\sigma H^T = S$. For a systematic encoder, the constant vector σ can always be chosen to be zero in its first k coordinates (thus a constant is added to the parity checks only).

Given a binary polynomial

$$g(x) = 1 + g_1 x + g_2 x^2 + \dots + g_{r-1} x^{r-1} + x^r,$$

of degree r , the power series

$$\frac{1}{g(x)} = (x) = \sum_{j=0}^{\infty} f_j x^j$$

is defined by the relationship

$$g(x)f(x) = 1.$$

Note that the power series $f(x)$ forms a periodic sequence, that is

$$\begin{aligned} f(x) &= f'(x) \sum_{i=0}^{\infty} x^{P_i} \\ 35 &= \frac{f'(x)}{1 - x^P}, \end{aligned}$$

where P is the (fundamental) period of $f(x)$ and

$$f'(x) = \sum_{j=0}^{P-1} f_j x^j$$

represents the truncated power series with P terms. It is well known that the maximum period $2^r - 1$ (thus $P \leq 2^r - 1$) is achieved if and only if $g(x)$ is a primitive polynomial; in this case, $f(x)$ is said to be a maximal length, pseudo-random (PN) sequence.

Closely associated with the power series $f(x)$ is the difference equation

$$\begin{aligned} y_j &= w_j - \sum_{i=1}^r g_i y_{j-i} \\ 55 &= \sum_{i=0}^{r-1} f_i w_{j-i}, \end{aligned}$$

which describes a linear, time-invariant, causal finite state system with input sequence w_j , output sequence y_j , and impulse response f_i .

60 Similarly, a rational function (i.e., ratio of polynomials)

$$\frac{a(x)}{g(x)} = a(x) = \sum_{j=0}^{\infty} a_j x^j$$

is defined by the polynomial equation

$$g(x)a(x) = a(x).$$

The power series $e(x)$ implies the difference equation

$$\begin{aligned} y_j &= \sum_{m=0}^{\text{degree}(a)} a_m w_{j-m} - \sum_{i=1}^r s_i y_{j-i} \\ &= \sum_{i=0}^r c_i w_{j-i}. \end{aligned}$$

If $f(x)=1/g(x)$ and $m \geq 0$ is any non-negative integer then the delayed power series ($c_j=f_j, m_j, j \geq 0$)

$$e(x) = \sum_{j=0}^{\infty} f_j x^j = \frac{a(x)}{g(x)}$$

for some $a(x)$ of degree less than r ($a(x)$ is easily determined from the polynomial equation $g(x)e(x)=a(x)$). Similarly, for the non-negative integer $k>0$ the truncated power series (a polynomial)

$$h^{k+1}(x) = \sum_{j=0}^k f_j x^j = \frac{a(x) - x^{k+1}b(x)}{g(x)}$$

for some $b(x)$ of degree less than r ($b(x)$ is easily determined from the polynomial equation $g(x)h^{k+1}(x)=a(x)-x^{k+1}b(x)$). The polynomial $h^{k+1}(x)=h_0+h_1x+h_2x^2+\dots+h_kx^k$ represents the truncated power series spanning the $k+1$ terms $\{f_m, f_{m+1}, f_{m+2}, \dots, f_{m+k}\}$, where $h_j=f_{m+j}$ for $j=0, 1, \dots, k$, and $h_j=0$ for $j>k$. The difference equation, in this case,

$$\begin{aligned} y_j &= \sum_{m=0}^{\text{degree}(a)} a_m w_{j-m} - \sum_{i=0}^{\text{degree}(b)} b_i w_{j-(i+1)-i} - \sum_{i=1}^r s_i y_{j-i} \\ &= \sum_{i=0}^k h_i w_{j-i} \end{aligned}$$

corresponds to a sliding window or finite impulse response (FIR) system. Note that this filter can be implemented (using the first difference equation) with a number of terms that has $\|a(x)\| + \|b(x)\| + \|g(x)\|$ terms rather than $\|h^{k+1}(x)\|$ terms (where $\|\cdot\|$ is the Hamming weight of the polynomial). This is very important in implementing the single bit in, single bit out decoder FIR filter (syndrome calculator) of the present invention since the polynomials $a(x)$, $b(x)$, $g(x)$ are small degree (8 or less) and the degree of $h^{k+1}(x)$ is large.

In implementing the present invention, it is desired to generate LBCs for which the parity check equations can be implemented by a single FIR filter. Let $h^{k+1}(x)$ be a polynomial of degree k with non-zero constant term ($h_0=h_k=1$). Then

$$H = \begin{pmatrix} h_k & h_{k-1} & \dots & \dots & \dots & h_0 & 0 & 0 & \dots & 0 \\ 0 & h_k & \dots & \dots & \dots & h_1 & h_0 & 0 & \dots & 0 \\ \vdots & \vdots & \ddots & & & \vdots & \vdots & \ddots & & \vdots \\ 0 & 0 & \dots & h_k & \dots & h_{k-1} & h_{k-2} & h_{k-3} & \dots & h_0 \end{pmatrix}$$

defines an FIR-parity-check LBC. With such an FIR-parity-check LBC, codewords, $C_i(x)$, that are concatenated together

$$w(x) = \sum_{i=0}^{\infty} c_i(x)x^i$$

can be synchronized by passing $w(x)$ through the FIR filter with response $h^{k+1}(x)$.

5 where each $y_i(x)$ has degree less than k . This is illustrated in FIG. 7, in which the c_i terms define successive codewords, each having n bits comprising k information bits and r parity bits. The codewords form a packet stream 120 with each packet comprising message bits m_i and parity bits p_i .

10 After processing by the syndrome calculator 122, a data stream 124 results in which each packet comprises the desired synchronization word s_i and the terms y_i , which are ignored.

The syndrome sequence $S(x)$ has the constant polynomial 15 $s(x)$ (a polynomial of degree less than r that determines which coset of the LBC is used) periodically embedded at the end of each n -block (in the absence of channel errors). Thus by correlating the syndrome sequence $S(x)$ with the constant polynomial $s(x)$, synchronization can be established and maintained. By using a systematic encoder, the 20 data is recovered directly from the concatenated sequence $w(x)$. Furthermore, once synchronization has been established, the syndrome can be used to detect errors in the data whenever the fixed polynomial $s(x)$ fails to appear at the anticipated time. Finally, by using an FIR parity check, the 25 syndrome former is self synchronizing (i.e., the initial conditions of the syndrome are resolved automatically) and has limited error propagation (the effect of an error is limited to the length of the FIR window, $K+1$ bits).

To choose the response $h^{k+1}(x)$, a recursive solution is 30 required. Once a recursion polynomial $g(x)$ is selected, a suitable $a(x)$ and $b(x)$ are determined so that

$$h^{k+1}(x) = \frac{a(x) - x^{k+1}b(x)}{g(x)}$$

35 with $h^{k+1}(x)$ having a non-zero constant term and degree k , with the first (h_0) and last (h_k) terms being 1 ($h_0=h_k=1$). Once $g(x)$ is specified, only certain choices of $a(x)$ and $b(x)$ will work.

40 FIG. 8 is a block diagram illustrating the components of the syndrome calculator and the synchronization detection. It is important to note that the effects of the initial conditions in the recursive portion of the circuit 122 (i.e., the feedback block 130 that implements the $1/g(x)$ function) have a finite 45 effect on the output. This is a direct consequence of the fact that the polynomial $f(x)=a(x)-x^{k+1}b(x)$ is divisible by $g(x)$ and that the operations that implement these functions operate on the output of the recursive part of the circuit. For example, if the initial conditions are non-zero in the $1/g(x)$ 50 circuit, and the input at terminal 126 is constantly zero, then the output of the recursive portion 130 is the pseudo random (PN) sequence generated by $1/g(x)$. However, within n steps, the output of the syndrome calculator will constantly produce zero at the output. This property also ensures that the 55 effects of channel errors on the output of the syndrome will be restricted to the $k+1$ span of the impulse response of the syndrome function.

As can be seen in FIG. 8, the syndrome calculator 122 implements the function $h^{k+1}(x)$ described above. The $a(x)$ 60 polynomial 134 and $b(x)$ polynomial 136 are added in exclusive-OR gate 140 to provide the actual syndromes. The input to the polynomial 136 is delayed by delay element 132.

The output of the syndrome filter is shifted into a register 65 150 of length r , where a match to the desired sync pattern $s(x)$ is made in comparator 152. The resultant sync signal is then used to establish and maintain synchronization as well as to detect the presence of errors.

Finally, a systematic encoder must be implemented. A simple two pass encoder can be implemented as follows. First, take the k bit message, followed by r zeros, and pass the resulting n bits through a syndrome calculator, producing an n bit output. Throw out the first k outputs and retain the last r bits. These r bits are then passed through a filter with response $g(x)/a(x)$ (this method assumes $k > r$). The r bits produced from this last filtering summed with a constant r bits (that determines $s(x)$) determine the parity bits that are to be transmitted. Note that there are simplifications that can be applied here. First, only the first $r-1$ message bits are needed for the "b(x)" polynomial, there is no need to build a buffer of length $k+1$ (as required at the receiver).

A common class of (n, k) LBCs used for error detection in a large variety of transmission and storage systems are the cyclic redundancy check (CRC) codes. These codes are best described in terms of polynomial codewords $c(x) \in F_2^n[x]$ (the set of binary polynomials of degree $< n$) and a generator polynomial $g(x)$ of degree $r = n - k$. The code

$$C = \{c(x) \in F_2^n[x] | c(x) = m(x)g(x), m(x) \in F_2^{n-r}[x]\}$$

is all polynomial multiples of the generator polynomial $g(x)$ of degree less than n . A CRC code can be described as an intersection of the ideal generated by $g(x)$ in the ring of polynomials $F_2[x]$.

$$\begin{aligned} C &= \langle g(x) \rangle \cap F_2^n[x], \langle g(x) \rangle = \{c(x) \in F_2[x] | c(x) = m(x)g(x), m(x) \in \\ &F_2^{n-r}[x]\}. \end{aligned}$$

Given the generator $g(x)$, of degree r , and the block length n for a CRC, one can always find polynomials $h(x)$, of degree $k = n - r$ and $f(x)$ of degree n such that $g(x)h(x) = f(x)$ and then

$$C = \{c(x) \in F_2^n[x] | c(x)h(x) = 0 \text{ modulo } f(x)\}.$$

C forms an ideal in the quotient ring $F_2[x]/\langle f(x) \rangle$. If one can solve $g(x)h(x) = x^n - 1$ (i.e., $f(x) = x^n - 1$) then the CRC is a cyclic code. In this case, the dual code is also a cyclic code with generator $x^k h(x^{-1})$

$$C^\perp = \langle x^k h(x^{-1}) \rangle \cap F_2^n[x]$$

and thus the dual of a cyclic code is a cyclic code. However, for most choices of block length n , it is not possible to solve $g(x)h(x) = f(x)$ with $f(x) = x^n - 1$. For example, if $g(x)$ is a primitive polynomial (or the product of a primitive polynomial with $x-1$, a common form of the generator used in many CRC codes), then the block length n must be divisible by $2^r - 1$ ($2^{r-1} - 1$). For such other values of n , the code C is in fact a shortened cyclic code since one can always find an integer $m \geq n$ such that $g(x)$ divides $x^m - 1$ and the code C is obtained by shortening the $(m, m-r)$ code $\langle g(x) \rangle \cap F_2^m[x]$ to the $(n, n-r)$ code $C = \langle g(x) \rangle \cap F_2^n[x]$.

For a shortened cyclic code, $m > n$, the polynomial $x^m h(x^{-1})$ does not generate the dual code and in fact the dual code is not the intersection with any ideal in $F_2[x]$. Thus the dual of a shortened cyclic code is not a shortened cyclic code.

As an example, consider the primitive polynomial $g(x) = 1 + x + x^2$ of degree $r = 3$ and the block lengths $n = 6, 7, 8$. In the following Table 2, the dimension of the code k is given as well as $f(x) = a(x)x^{r-1}b(x) = g(x)h(x)$ and the value of the smallest cyclic code length m .

TABLE 2

n	k	a(x)	b(x)	f(x)	h(x)	m
6	3	$1+x$	$1+x^2$	$1+x+x^2+x^4$	$1+x^2$	7
7	4	1	x^2	$1+x^3$	$1+x+x^2+x^4$	7
8	5	$1+x$	x^2	$1+x^2+x^4$	$1+x^2$	14

$$g(x) = 1 + x + x^2, n = 6, 7, 8$$

Notice that only in the case $n=7$ is the code a cyclic code which has a dual that is itself a cyclic code. In the other two cases, $n=6, 8$ the codes are shortened cyclic codes which have duals that are not shortened cyclic codes.

In connection with the present invention, it has been realized that for reasons of simplifying the syndrome calculation, the dual of a shortened cyclic code offers distinct advantages over the usual CRC technique of using a shortened cyclic code. Thus for example, once $g(x)$ and n have been fixed, the codewords of a CRC would be the set $C_{CRC} = \langle g(x) \rangle \cap F_2^n[x]$ while the illustrated implementation of the present invention uses the set $C_{FIR-P-C} = \langle x^k h(x^{-1}) \rangle \cap F_2^n[x]$.

$F_2^n[x]$)¹. Note that $C_{FIR-P-C} = C_{CRC}$ unless the code is a cyclic code (i.e., $g(x)$ divides $x^n - 1$). The choice of $C_{FIR-P-C}$ means that the simple syndrome calculation procedure described previously will apply. This would not be possible in general with C_{CRC} .

In an MPEG implementation as illustrated in FIGS. 3-6, the packets are 188 bytes ($n=1504$ bits) long with 187 bytes ($k=1496$ bits) of data and 1 byte ($r=8$ bits) of sync word. (Note that $2^8 = 1 = 255$ does not divide $n=1504$). The illustrated embodiment uses the space for the 1 byte sync word to accomplish both synchronization and additional error detection, above that provided by other error detection layers in the transmission system, such as Reed Solomon encoding. This is accomplished via an FIR-parity-check based linear block code, as described above. The parameters of one possible code are ($n=1504$, $k=1496$) where:

$$g(x) = 1 + x + x^2 + x^4 + x^8;$$

$$a(x) = 1;$$

$$b(x) = 1 + x + x^2 + x^7,$$

which is based on a primitive polynomial $g(x)$ of degree 8 (i.e., it produces a PN-sequence of length 255), a constant $a(x)$ and a $b(x)$ with 4 terms.

The system uses a coset of the FIR-parity-check LBC. The sequence chosen $s(x) = 1 + x + x^2 + x^6$ (0x47 in Hex) has good auto-correlation properties and, advantageously, the same as the conventional MPEG sync word. This result is achieved by adding the offset $o(x) = 1 + x + x^2 + x^5 + x^6$ (0x67 in Hex) to the parity check byte at the transmitter.

It should now be appreciated that the present invention provides a method and apparatus for achieving synchronization and detecting errors in a packetized data stream. Although the invention has particular applicability to the synchronization and error detection in an MPEG transport packet scheme, it is not limited to use with the MPEG format. The invention also provides a unique and economical decoder, in which syndrome calculation is accomplished using a one bit input, one bit output FIR filter. An advantageous class of codes which can be used to generate the parity bits used for the checksum in accordance with the present invention is the class of linear block codes which are duals of shortened cyclic codes.

The inclusion of a parity checksum encoding layer affords a substantial improvement in the error detection capability

of the transmission system. A conventional error correction layer (such as a Reed-Solomon layer) alone will detect errored data approximately 85% of the time, whereas the checksum of the present invention alone will provide a detection rate of 99.6%. Combining both detection mechanisms will yield an overall detection rate of 99.94%. This is an important consideration when the system relies on the concealment of errors when operating in high noise environments.

An additional advantage of this encoding scheme is an improvement in the reliability with which packet synchronization is accomplished. The standard sync word approach is vulnerable to repetitive data patterns within the packets

which might be falsely acquired as the sync word location. A large measure of this data dependence is removed in the method and apparatus of the present invention by encoding the data itself to provide the synchronization information.

Although the invention has been described in connection with various specific embodiments, it should be understood and appreciated that numerous adaptations may be made thereto without departing from the spirit and scope of the invention, as set forth in the claims. For example, the following additional sets of parity check polynomials (or others) could be used in connection with ($n=1504$, $k=1496$) codes:

Table 1: Error probability bounds for ($n = 1504$, $k = 1496$) codes

Selected Parity Check Polynomials for $n = 10$

We claim:

1. A method for achieving synchronization and detecting errors in a data stream carrying successive packets of k bits or each packet comprising a variable pattern, comprising the steps of:

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locating at least one synchronization pattern in said data stream to enable the boundaries for the k information bits of successive packets to be determined;

replacing the synchronization pattern in each packet with an r-bit parity code derived from a counterpart set of k information bits in said data stream, thereby generating a modified data stream;

communicating said modified data stream to a decoder;

locating at least one of said parity codes in said modified data stream at said decoder to achieve synchronization, thereby enabling the boundaries for the k information bits of successive packets to be determined; and

comparing said parity codes to checksums obtained from their counterpart k information bits at said decoder to determine when the information bits in a packet contain an error.

2. A method in accordance with claim 1 wherein:

the synchronization pattern for each packet precedes the k information bits of that packet; and

the counterpart set of k information bits for each parity code comprises the k information bits immediately preceding the parity code.

3. A method in accordance with claim 1 wherein said parity code is generated from a linear block code comprising a dual of a shortened cyclic code.

4. A method in accordance with claim 1 wherein said data stream is an MPEG compatible data stream.

5. A method in accordance with claim 4 comprising the further step of scaling said parity codes such that when decoded at said decoder, they will match MPEG synchronization patterns.

6. A method in accordance with claim 4 wherein k=1496.

7. Communication apparatus for enabling a receiver to robustly obtain synchronization and detect errors in a data stream carrying successive packets of k information bits and an r-bit parity code, the parity code of each packet comprising a predefined pattern of bits detectable at said receiver by searching for said pattern and functioning as a checksum for information bits carried in said data stream, said apparatus comprising:

means for inserting the parity codes in said packets prior to communication to said receiver, each of said parity codes being derived from a counterpart set of k information bits in said data stream;

means for communicating said data stream to said receiver after insertion of said parity codes;

means for locating at least one parity code in said data stream at said receiver to achieve synchronization, thereby enabling the boundaries for the k information bits of successive packets to be determined; and

means at said receiver for comparing said parity codes to checksums obtained from their counterpart k information bits to determine when the information bits in a packet contain an error.

8. Apparatus in accordance with claim 7 further comprising:

a parity check matrix at said receiver for generating a predefined synchronization pattern from valid parity codes.

9. Apparatus in accordance with claim 8 wherein said predefined synchronization pattern is a standard MPEG synchronization pattern.

10. Apparatus in accordance with claim 7 wherein said data stream contains synchronization patterns prior to insertion of said parity codes, said apparatus further comprising:

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means for replacing said synchronization patterns with said parity codes to provide a modified data stream for communication to said receiver.

11. Apparatus in accordance with claim 10, further comprising:

means at said receiver for reconstructing said data stream from said modified data stream by replacing said parity codes with said synchronization patterns.

12. Apparatus in accordance with claim 10 wherein:

each packet commences with one of said synchronization patterns, with the k information bits for the packet following the synchronization pattern for that packet; and

each synchronization pattern is replaced with a parity code derived from the k information bits of the preceding packet.

13. Apparatus in accordance with claim 12 wherein said data stream is an MPEG compatible data stream.

14. Apparatus in accordance with claim 13 further comprising:

means for scaling said parity codes such that when decoded at said receiver, they will match an MPEG synchronization pattern.

15. A decoder for a packetized digital data stream in which successive packets each contain k information bits and an r-bit parity code, the parity code of each packet being derived from k bits of information carried by said data stream, comprising:

means for searching said data stream during a signal acquisition phase to locate a parity code contained therein;

means for establishing a synchronization condition based on one or more parity codes located by said searching means;

means for comparing a checksum derived from the k information bits of each packet to the parity code for those k information bits during a tracking phase; and

means for signalling an error in the k information bits for a packet when the checksum for those bits does not match the parity code therefor.

16. A decoder in accordance with claim 15 wherein:

the parity code is derived from the k information bits of the immediately preceding packet.

17. A decoder in accordance with claim 15 wherein said parity codes are generated from a linear block code comprising a dual of a shortened cyclic code.

18. A decoder in accordance with claim 15 wherein said data stream is encoded in an MPEG compatible format, said decoder further comprising:

means for replacing the parity code in each packet with an MPEG synchronization pattern.

19. A decoder in accordance with claim 15 further comprising:

means for monitoring said parity codes during said tracking phase; and

means responsive to said monitoring means for switching from said tracking phase to said acquisition phase after a predetermined plurality of r-bit patterns considered by said monitoring means to be parity codes are found to be invalid.

20. A decoder in accordance with claim 19 wherein said data stream is encoded in an MPEG compatible format, said decoder further comprising:

means for replacing the parity code in each packet with an MPEG synchronization pattern.

21. A decoder in accordance with claim 20 wherein:
 each parity code is derived from the k information bits of
 the immediately preceding packet; and
 each synchronization pattern comprises the first r bits in 5
 a packet and is followed by the k information bits for
 that packet.
22. Apparatus for calculating syndromes for linear block
 coded codewords, comprising:
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 a finite impulse response filter having an input for receiv-
 ing a serial bit stream of codeword data, each codeword
 containing k information bits and r parity bits, said filter
 having an output for providing a serial bit stream of
 syndromes, said syndromes comprising a fixed linear
 combination of a current bit of said codeword data
 input to said filter and the k previous bits of said
 codeword data;
 15
 wherein said filter has an impulse response $h^{k+1}(x)$, 20
 where:

$$h^{k+1}(x) = \frac{a(x) - x^{k+1}b(x)}{g(x)},$$

g(x) is a generator polynomial of degree r describing a recursion to provide an infinite impulse response, and a(x) and b(x) are polynomials chosen such that the polynomial $h^{k+1}(x)$ will be of degree k, have a non-zero constant term $h_0=1$, and have a non-zero final term $h_k=1$ to provide finite impulse responses.

23. Apparatus in accordance with claim 22 wherein said linear block code is a dual of a shortened cyclic code.
24. Apparatus in accordance with claim 22 further comprising:
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 means coupled to the output of said filter for detecting a synchronization pattern in the serial bit stream of syndromes.

* * * * *

EXHIBIT D



US005745522A

United States Patent [19]
Heegard

[11] Patent Number: **5,745,522**
[45] Date of Patent: **Apr. 28, 1998**

[54] RANDOMIZER FOR BYTE-WISE SCRAMBLING OF DATA

[75] Inventor: Chris Heegard, Ithaca, N.Y.

[73] Assignee: General Instrument Corporation of Delaware, Chicago, Ill.

[21] Appl. No.: 556,415

[22] Filed: Nov. 9, 1995

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H04L 27/30

[52] U.S. Cl. 375/208; 380/9; 380/46;
364/717.03

[58] Field of Search 331/78; 375/200,
375/208; 364/717.03, 746.1; 380/9, 47,
46; 370/515

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Primary Examiner—Stephen Chin

Assistant Examiner—Bryan Webster

Attorney, Agent, or Firm—Barry R. Lipsitz; Ralph F. Hoppin

[57] ABSTRACT

An N-bit, byte-wise data randomizer uses a linear feedback shift register arrangement where each register stage stores N-bits. In this manner, a pseudorandom sequence can be generated based on a nonbinary primitive polynomial over a finite field of any desired length. In a specific disclosed embodiment, the primitive, degree three trinomial

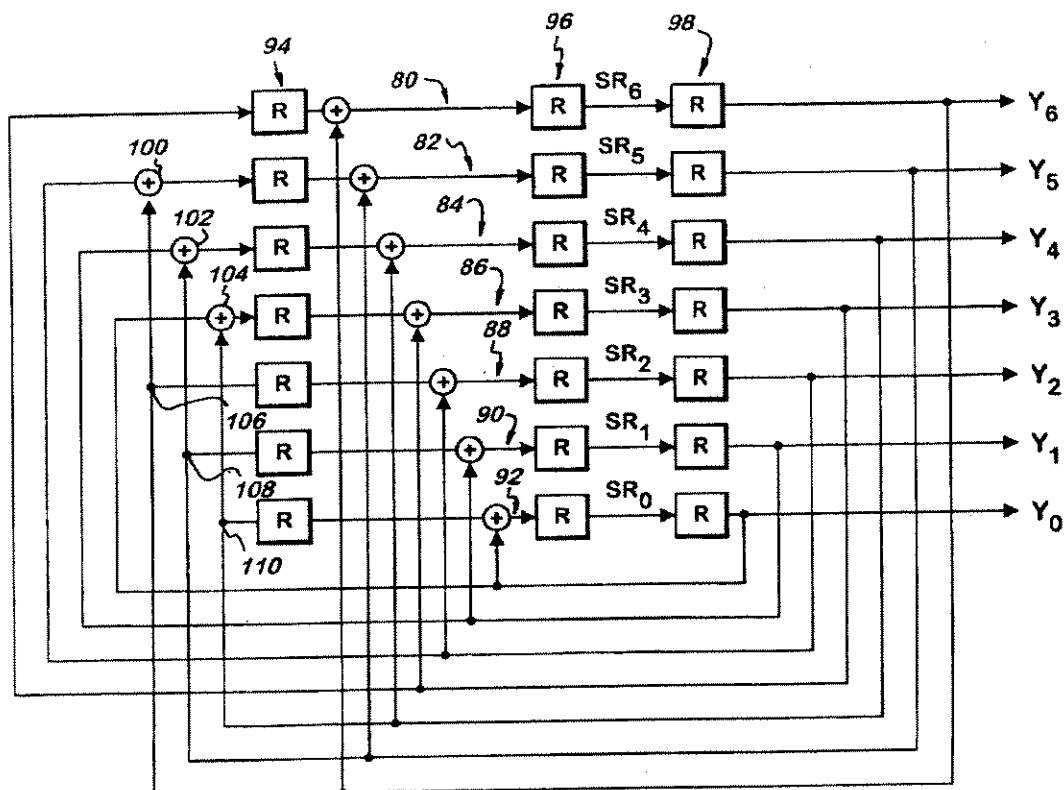
$$f(x)=x^3+x+1$$

over the finite field

$$F_{128}=F_3(\alpha)/(x^7+x^3+1)$$

is implemented.

15 Claims, 2 Drawing Sheets



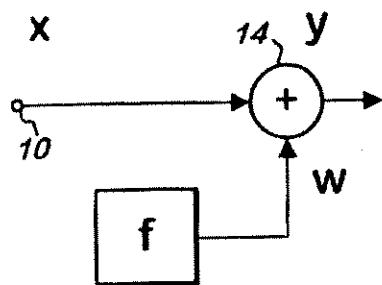


Fig. 1

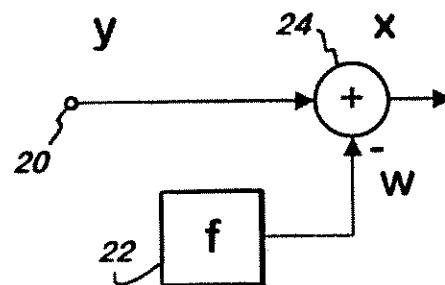


Fig. 2

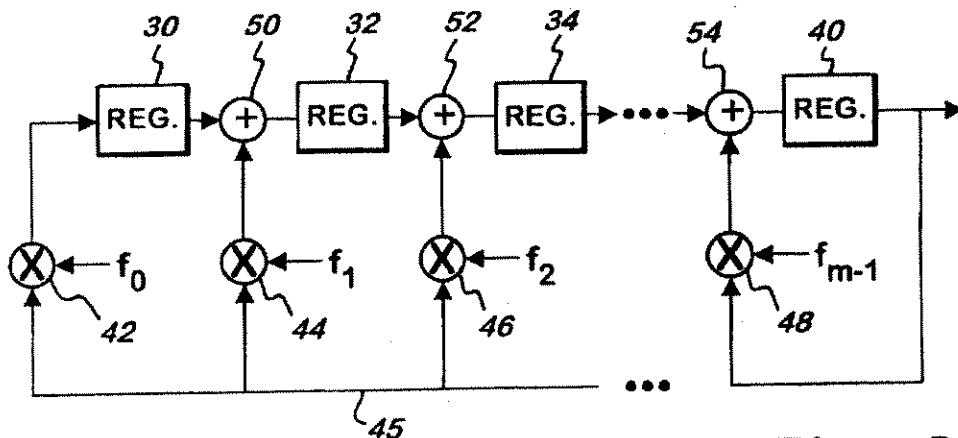


Fig. 3

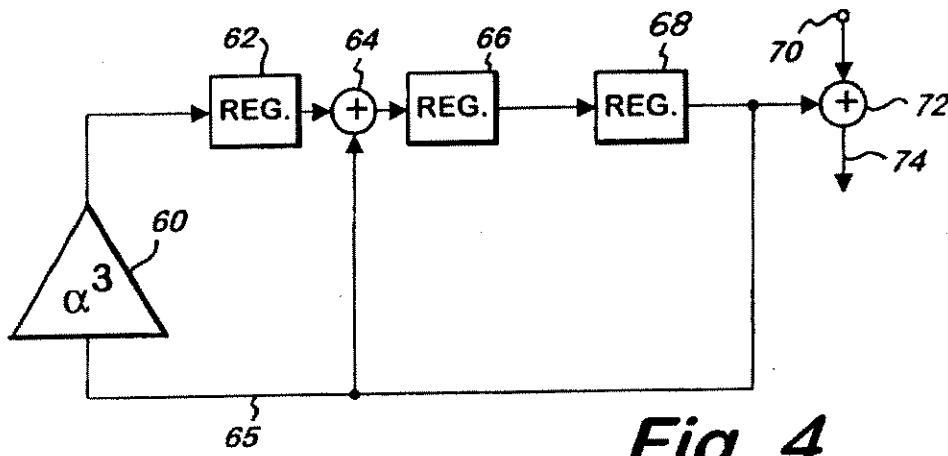
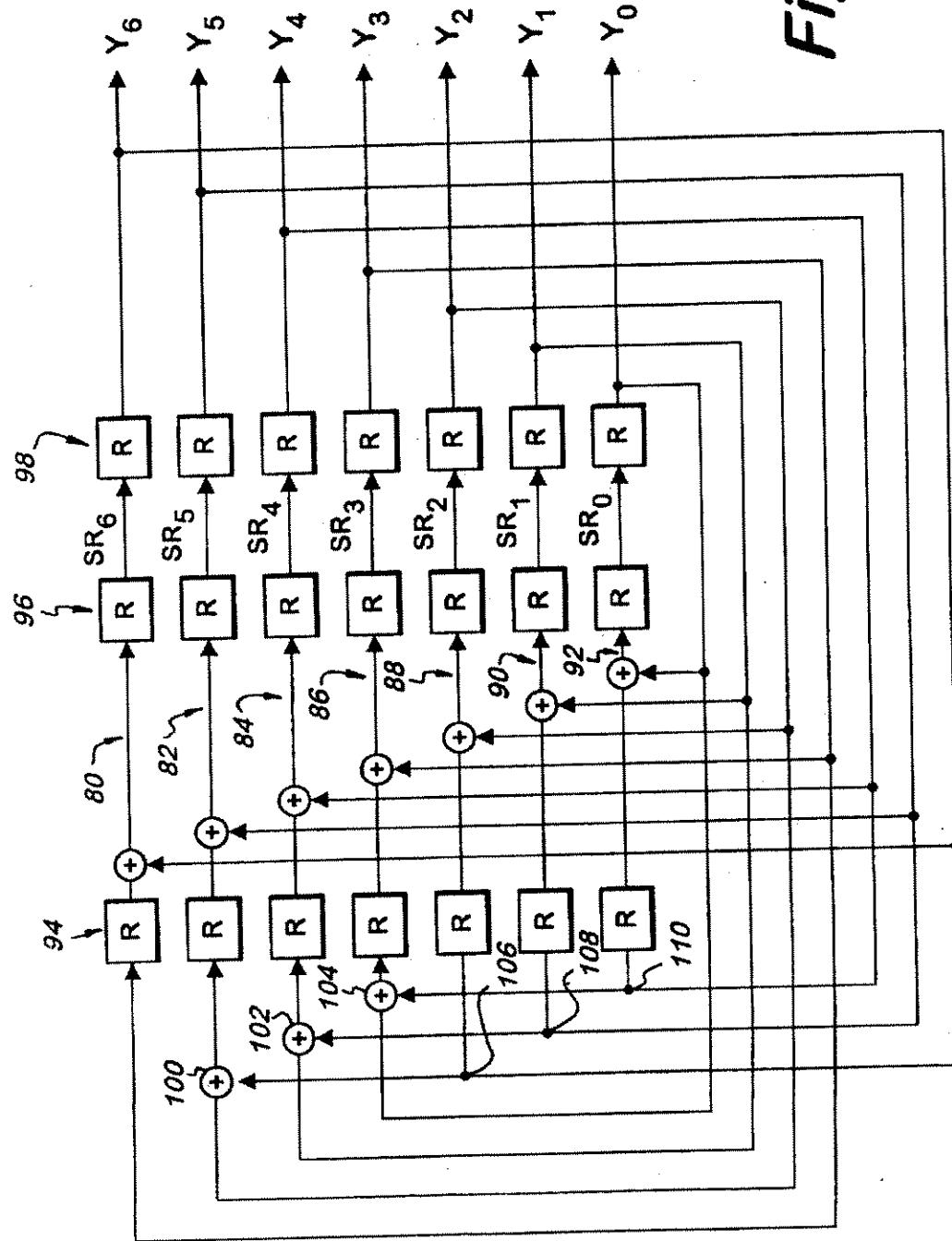


Fig. 4

Fig. 5



RANDOMIZER FOR BYTE-WISE SCRAMBLING OF DATA

BACKGROUND OF THE INVENTION

The present invention relates to digital communication, and more particularly to a data randomizer for use with a QAM modem or the like.

In order to transmit information across a communication path such as a cable television path or telephone line, the information is typically modulated on a carrier. At a receiver, the information must be demodulated from the carrier. Modems are devices which modulate and demodulate information transmitted on and received from a communication path. Modems have evolved from early schemes using frequency shift keying (FSK) at 300 bits per second (BPS) to those using quadrature amplitude modulation (QAM) at rates of 28,800 BPS or higher over a telephone line.

It is conventional to scramble a data stream before it is input to a modem using a binary linear feedback shift register (LFSR) in order to assist in the recovery of the carrier and clock at a receiver. Bit-wise LFSR structures are well known in the art. See, for example, B. Sklar, Digital Communications, Prentice Hall, Englewood Cliffs, N.J., 1988, pp. 547-548 and 694-695. Scrambling, or randomization of the data stream input to a modem is intended to prevent long sequences of logical "1"s or "0"s. The scrambler performs a logical operation on the data bits to be transmitted using a polynomial with binary coefficients implemented via the LFSR. Descrambling is carried out using a circuit that performs the inverse operation using the same polynomial.

The scrambler produces a pseudorandom noise (PN) sequence which is exclusive-OR'd with the transmitted signal to ensure a random transmitted sequence. Such a scrambling approach is particularly applicable when synchronization information is available to the descrambler.

In implementing a binary scrambler using an LFSR, it is advantageous to use a "primitive polynomial," which is one that will result in a maximum length PN sequence for a given length of polynomial. If the LFSR implements a primitive polynomial, then the PN sequence output from the LFSR will comprise a maximum length sequence of length $2^m - 1$, where m is the number of LFSR stages (i.e., the "length" of the LFSR and the degree of the binary polynomial). In designing such a scrambler, polynomials with only a few nonzero coefficients are of particular interest in order to reduce hardware complexity. For example, a polynomial with three nonzero terms (i.e., a "trinomial") can provide a particularly advantageous and cost effective scrambler implementation.

The present invention provides a scrambler/descrambler having the aforementioned and other advantages. More particularly, the present invention provides a data randomizer/derandomizer for scrambling/unscrambling data bytes on a "byte-wise" level, wherein data is input to the randomizer or derandomizer a byte at a time, and the bits within the byte are scrambled concurrently.

SUMMARY OF THE INVENTION

The present invention provides a data randomizer for processing bytes of data to scramble data bits contained therein. It should be appreciated that the randomizer can also be used to derandomize (i.e., descramble) data that has already been randomized by a counterpart randomizer. Thus, the term randomizer as used herein and in the claims is intended to also encompass a derandomizer.

Each byte of data processed by the randomizer has an integer number N of bits. The randomizer comprises a linear feedback shift register (LFSR) having a plurality of register stages in series. Each stage is capable of storing an N -bit byte. The LFSR includes at least one feedback tap for implementing a primitive polynomial of degree M over a finite field of size $q=2^N$. Means are provided for multiplying an N -bit pseudorandom output from the LFSR by an N -bit value f_k that is an element of the finite field. The multiplying means are coupled to input the product of the multiplication into a stage of the LFSR.

In an illustrated embodiment, each of the data randomizer register stages comprises N binary registers in parallel. Each of the N registers of a register stage has a counterpart register in the other register stages.

In a specific implementation, $N=7$ and a primitive polynomial of degree $M=3$, over the finite field with 128 elements is the polynomial

$$f(x)=x^3+x+\alpha^2$$

where α^2 is a value in the field and α is a primitive element of the field. The "minimal polynomial" for α (a binary primitive polynomial) is the binary polynomial x^7+x^3+1 .

In an illustrated embodiment, a data randomizer is provided for scrambling seven-bit data bytes. The randomizer comprises a bank of seven linear feedback shift registers SR_0-SR_6 for providing an output seven pseudorandom (PN) sequences Y_0-Y_6 , respectively. Each of the LFSRs comprise three register stages in series and have feedback taps after the first and third stages to represent the trinomial $f(x)=x^3+x+\alpha^2$. The PN sequences Y_0-Y_6 from the third stages of the LFSRs are fed back to the tap that follows the first stage of the respective LFSR. The first stage of LFSRs SR_6, SR_5, SR_4, SR_3 , and SR_2 receive as inputs the PN sequences Y_3, Y_4, Y_5 , and Y_6 , respectively. The first stage of LFSRs SR_3, SR_4 , and SR_5 receive as inputs the exclusive-ORs $Y_0 \oplus Y_4, Y_1 \oplus Y_5$, and $Y_2 \oplus Y_6$, respectively.

The data randomizer can further comprise an exclusive-OR gate following each LFSR for exclusive-ORing the PN sequence from that LFSR with a respective bit of a seven-bit data byte to be scrambled.

Each of the LFSRs is initialized using a nonzero initialization state.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a generalized block diagram of a synchronized scrambler;

FIG. 2 is a generalized block diagram of a synchronized unscrambler (also referred to as "descrambler");

FIG. 3 is a block diagram of a linear shift register PN generator;

FIG. 4 is a symbol-level block diagram of a byte scrambler in accordance with the present invention; and

FIG. 5 is a bit-level block diagram of a seven-bit byte scrambler in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 illustrates in block diagram form the general concept of a synchronized scrambler for randomizing data X input via terminal 10. The conventional case of such a scrambler involves a binary sequence. A scrambling function 12 which can comprise, for example, a polynomial implemented in a linear feedback shift register, is exclusive-OR'd with the input data X in XOR gate(s) 14. The XOR

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gate(s) 14 provides a binary addition. The function f provides a pseudorandom noise sequence W which, when exclusive-OR'd with the input data X, provides randomized data y at the output of XOR gate(s) 14.

FIG. 2 is a block diagram of a generalized descrambler that performs the inverse operation of the scrambler illustrated in FIG. 1. The randomized data y is input to XOR gate(s) 24 via terminal 20. Function 22, which is the same as function 12 illustrated in FIG. 1, provides the pseudorandom output W which, when exclusive-OR'd with the scrambled data y, produces the original data X assuming there are no errors in the received data y. As indicated, the XOR gate(s) 24 provides a binary subtraction.

FIG. 3 illustrates a linear shift register PN generator. The conventional case of such a PN generator involves a binary sequence. An autonomous LFSR is a clock synchronous shift register augmented with appropriate feedback taps and receiving no external input. It performs as a serial linear finite state machine, where the memory cells are simple D flip-flops and the next state operations are implemented solely by exclusive-OR gates. In the LFSR illustrated in FIG. 3, each register stage 30, 32, 34 . . . 40 can be implemented using a D flip-flop. Coefficients $f_0, f_1, f_2, \dots, f_{m-1}$ of the specific polynomial to be implemented are input via corresponding multipliers 42, 44, 46 . . . 48. Taps, such as taps 50, 52 and 54 are provided for all nonzero coefficients in order to implement the polynomial. In the event taps are provided for any zero value coefficients, they will not be utilized since the respective coefficient input will be zero.

A binary LFSR of length m can be described by a polynomial with binary coefficients of degree m, where the nonzero coefficients of the polynomial denote the positions of the respective feedback taps. The state of the LFSR is denoted by the binary state of its cells. If the LFSR is initialized in a nonzero state, it cycles through a sequence of states and eventually comes back to the initial state, following the functionality of the next state rules implemented by its polynomial description. An LFSR that goes through all possible $2^m - 1$ nonzero states is said to be described by a "primitive" polynomial.

The present invention provides both a generalized byte-wise randomizer and a specific data randomizer. The specific implementation disclosed scrambles seven-bit data bytes used in a communication system (e.g., a digital cable television system) having Reed-Solomon (R/S) forward error correction and interleaving that is synchronized using a sync pattern. In particular, the communication system in which the data randomizer of the present invention is used inserts the sync pattern after every 60 R/S codewords. Each codeword is 128 symbols long, with seven bits per symbol. This amounts to a total of 7,680 symbols which is equivalent to 53,760 bits.

The most common method of PN generation is to generate a sequence using a binary, linear feedback shift register specified by a binary polynomial

$$f(x) = f_0 + f_1 x + \dots + f_m x^m,$$

where

$$f_i \in \{0, 1\} (f_m \neq 1).$$

If the polynomial is a primitive polynomial, then the generator produces a maximum length sequence of length $2^m - 1$. Polynomials with only a few nonzero coefficients are of particular interest, since they can be implemented using less

hardware than polynomials with many nonzero coefficients. A polynomial with three nonzero terms, referred to as a trinomial, can be implemented in a linear feedback shift register (LFSR) having only three shift register stages per bit.

Primitive polynomials are well known from Galois field theory. The construction of a Galois field is well known from the literature, and is described in detail, for example, in Lin and Costello, Jr., *Error Control Coding*, Prentice-Hall, 1983, pp. 29-40.

The theory of PN sequences and primitive polynomials extends to other finite fields F_q . For example, the finite field with 128 elements (corresponding, e.g., to a 128 symbol R/S codeword) is generated by the irreducible polynomial

$$f(x) = x^7 + x^3 + 1.$$

This trinomial is a primitive polynomial and will generate a binary pseudorandom sequence of length 127, which is the maximum possible period ($2^m - 1$). If $\alpha \in F_{128}$ is a root, $f(\alpha) = 0$, then β is called a primitive element of the field and $\alpha^7 = \alpha^3 + 1$.

A pseudorandom sequence over a finite field F_q can be generated by a polynomial with coefficients over the field. Again, if the polynomial is primitive, the length of the sequence is maximum ($q^m - 1$). For example, for a third degree polynomial over F_{128} , a primitive polynomial will generate a sequence of seven-bit symbols of length

$$(2^7)^2 - 1 = (2^{14} - 1) = 2,097,151.$$

The present invention extends the conventional binary implementation of an LFSR randomizer to a nonbinary implementation, wherein a primitive polynomial over a finite field F_q , $q > 2$, is used. An example implementation of such a randomizer is illustrated in FIGS. 4 and 5. In the specific embodiment illustrated, a primitive, degree 3 trinomial over the finite field

$$F_{128} = F_2[\alpha] / (\alpha^7 + \alpha^3 + 1)$$

is implemented. The polynomial

$$f(x) = x^3 + x + \alpha^2$$

has only one nonzero coefficient that is not one. This is the α^2 term, which is a non-zero constant that is an element of F_{128} .

In FIG. 4, the constant α^2 designated by box 60 multiplies the bits fed back on path 65 prior to shifting the feedback bits into first register 62. Register 62 stores a seven-bit value in the case where a finite field with 128 elements (F_{128}) is implemented. Thus, seven-bit bytes can be processed on a byte-wise level, instead of on a bit-wise level as in prior art randomizers. Since the randomizer of FIG. 4 implements a trinomial having nonzero values only for the x^3 , x and constant terms, taps are provided only after register 62 (the x term) and register 68 (the x^3 term). The tap after register 62 is implemented by XOR gate(s) 64. The output of register 68 is fed back via the constant term α^2 to register 62. There is no tap after register 66, which corresponds to the x^2 term that has a zero coefficient in the polynomial

$$f(x) = x^3 + x + \alpha^2$$

As indicated above, it should be appreciated that each of registers 62, 66 and 68 store seven bits at a time, to implement a byte-wise randomizer for processing data in seven-bit data bytes. This differs from prior art devices implementing binary fields and using single-bit registers.

The output of register 68 is a pseudorandom sequence of maximum length $q^m - 1$ which, in the case where $m=3$ and $q=128$, corresponds to a maximum length sequence of 2,097,151. This pseudorandom sequence is exclusive-OR'd with data input via terminal 70 to be scrambled. The output of the XOR gate(s) 72 on line 74 comprises the scrambled data.

FIG. 5 is a bit level circuit description of the symbol level block diagram of FIG. 4. Register stages 94, 96 and 98 each include seven separate registers "R" residing in parallel paths 80, 82, 84, 86, 88, 90 and 92. Thus, each register stage 94, 96, 98 is capable of storing a seven-bit byte. As in the symbol level implementation of FIG. 4, taps are provided after the x register stage 94 and the x^3 register stage 98. The constant term α^3 is implemented using exclusive-OR gates 100, 102 and 104 as well as the connections 106, 108 and 110 illustrated into the respective registers of register stage 94. For the bank of seven linear feedback shift registers 80-92 (SR₀-SR₆) illustrated in FIG. 5, seven binary pseudorandom sequences Y_0-Y_6 are generated. Each of these binary PN sequences is fed back to the tap that follows the register 94 of the respective LFSR. The first stage of LFSRs SR₀, SR₁, and SR₂ receive as inputs the PN sequences Y₃, Y₄, Y₅, and Y₆, respectively. The first stage of LFSRs SR₃, SR₄, and SR₅ receive as inputs the exclusive-OR's Y₀ \ominus Y₄, Y₁ \ominus Y₅, and Y₂ \ominus Y₆, respectively. Prior to using the randomizer of FIG. 5, each of the registers in register stages 94, 96 and 98 will be initialized with a definite, nonzero, initial state. For example, each register can be initialized with a binary "1".

Although the implementations of FIGS. 4 and 5 are directed specifically to the trinomial

$$f(x)=x^3+x+\alpha^3$$

which is particularly useful for the finite field of

$$F_{128}=F_2[\alpha]/(x^3+\alpha^3+1),$$

it should be appreciated that the inventive concept can be used to implement a randomizer for any nonbinary polynomial over a finite field of any possible length. The particular implementation illustrated is particularly suitable for randomizing 128 symbol long Reed-Solomon codewords, where each symbol comprises seven bits.

Although the invention has been described in connection with a specific illustrative embodiment, those skilled in the art will appreciate that numerous adaptations and modifications may be made thereto without departing from the spirit and scope of the invention, as set forth in the claims.

I claim:

1. A data randomizer for processing bytes of data to provide byte-wise scrambling of data bits therein, each byte having an integer number N of bits, said randomizer comprising:

a linear feedback shift register (LFSR) having a plurality of register stages in series, each stage capable of storing an N-bit byte, said LFSR including at least one feedback tap for implementing a primitive polynomial of degree M over a finite field of size 2^N ; and

means for multiplying an N-bit pseudorandom output from said LFSR by an N-bit value f_k that is an element of said finite field, said multiplying means being coupled to input a product produced thereby into at least one stage of said LFSR.

2. A data randomizer in accordance with claim 1 wherein each of said register stages comprises N registers in parallel.

3. A data randomizer in accordance with claim 2 wherein each of the N registers of a register stage has a counterpart register in the other register stages.

4. A data randomizer in accordance with claim 3 wherein N=7, M=3 and said primitive polynomial of degree M=3 is the polynomial f(x)=x³+x+ α^3 , where α^3 is said N-bit value of said finite field satisfying

$$\alpha^7+\alpha^3+1=0.$$

5. A data randomizer in accordance with claim 1 wherein N=7, M=3 and said primitive polynomial of degree M=3 is the polynomial f(x)=x³+x+ α^3 , where α^3 is said N-bit value of said finite field satisfying $\alpha^7+\alpha^3+1=0$.

6. A data randomizer for scrambling seven-bit data bytes, said randomizer comprising:

a bank of seven linear feedback shift registers SR₀-SR₆ for providing as output seven binary pseudorandom (PN) sequences Y₀-Y₆, respectively;

each of said linear feedback shift registers ("LFSRs") comprising three register stages in series and having feedback taps after said first and third register stages; the PN sequences Y₀-Y₆ from the third stages of the LFSRs being fed back to the tap that follows the first stage of the respective LFSR;

the first stage of LFSRs SR₀, SR₁, and SR₂ receiving as inputs the PN sequences Y₃, Y₄, Y₅, and Y₆, respectively; and

the first stage of LFSRs SR₃, SR₄, and SR₅ receiving as inputs the exclusive-OR's Y₀ \ominus Y₄, Y₁ \ominus Y₅, and Y₂ \ominus Y₆, respectively.

7. The data randomizer of claim 6 further comprising:

an exclusive-OR gate following each LFSR for exclusive-OR'ing the PN sequence from that LFSR with a respective bit of a seven-bit data byte to be scrambled.

8. The data randomizer of claim 7 wherein each of said LFSRs is initialized using a nonzero initialization state.

9. The data randomizer of claim 8 wherein said initialization sequence comprises the state 1.

10. The data randomizer of claim 6 wherein each of said LFSRs is initialized using a nonzero initialization state.

11. The data randomizer of claim 10 wherein said initialization sequence comprises the state 1.

12. A method for byte-wise randomizing of N-bit bytes of data comprising the steps of:

generating N pseudorandom sequences in parallel each over a finite field F_q specified by a nonbinary primitive polynomial with coefficients over the field, where q=2^N; and

exclusive-ORing a next successive bit from each of said N pseudorandom sequences with a corresponding bit of a next successive N-bit byte to randomize said byte.

13. A method in accordance with claim 12 wherein N=7 and said nonbinary primitive polynomial comprises the trinomial f(x)=x³+x+ α^3 over the finite field F₁₂₈=F₂[\alpha]/(x³+ α^3 +1).

14. A method in accordance with claim 13 comprising the further step of initializing said pseudorandom sequence with a non-zero initial state.

15. A method in accordance with claim 12 comprising the further step of initializing said pseudorandom sequence with a nonzero initial state.

EXHIBIT E



US005751373A

United States Patent [19]

Ohyama et al.

[11] Patent Number: 5,751,373
 [45] Date of Patent: May 12, 1998

[54] TELEVISION FUNCTION SELECTION METHOD, TELEVISION RECEIVER AND REMOTE COMMANDER FOR TELEVISION RECEIVER

[75] Inventors: Tomoko Ohyama, Kanagawa; Yukiko Ohkura, Tokyo; Masaharu Fukumoto; Shigeyuki Sano, both of Kanagawa; Yasuko Rokukawa, Tokyo; Shiro Endo, Chiba; Kyosuke Oda; Yumiko Minakawa, both of Kanagawa; Chifumi Matsunaga, Tokyo, all of Japan

[73] Assignee: Sony Corporation, Tokyo, Japan

[21] Appl. No.: 623,112

[22] Filed: Mar. 28, 1996

[30] Foreign Application Priority Data

Mar. 31, 1995 [JP] Japan 7-074892

[51] Int. Cl⁶ H04N 5/445

[52] U.S. Cl. 348/569; 348/734; 348/564

[58] Field of Search 348/563, 564, 348/569, 725, 734, 589, 600; H04N 5/445, 5/50, 9/74, 9/76

[56] References Cited

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Primary Examiner—Sherrie Hsia
 Attorney, Agent, or Firm—Jay H. Maioli

[57] ABSTRACT

A method and apparatus by which function as of a television receiver can be selected simply. A main menu displays the highest level of a hierarchical menu which includes items corresponding to functions of a television receiver is displayed on a left side portion of a screen of the television receiver. When a cursor is moved to the first item of the main menu, while the main menu remains displayed on the screen, a sub menu corresponding to the first item is displayed on a right side portion of the screen. When the cursor is subsequently moved to one of the items forming the sub menu and then a predetermined operation is performed.

13 Claims, 22 Drawing Sheets

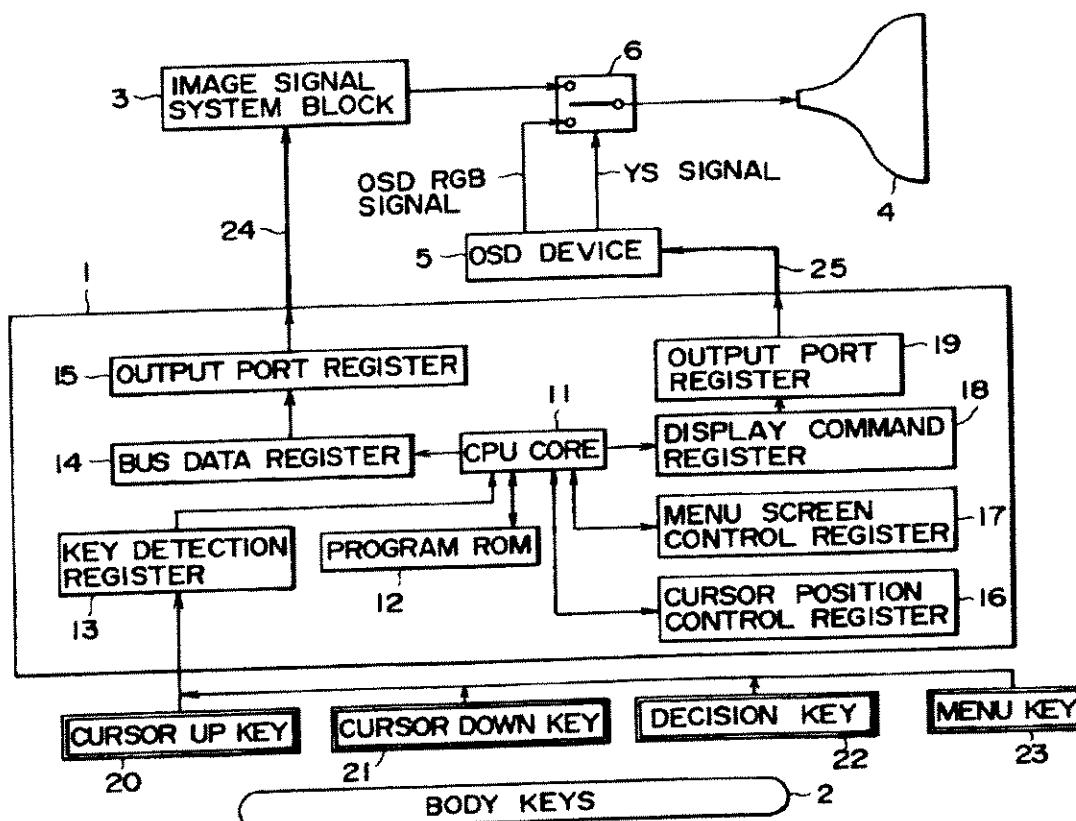


FIG. 1

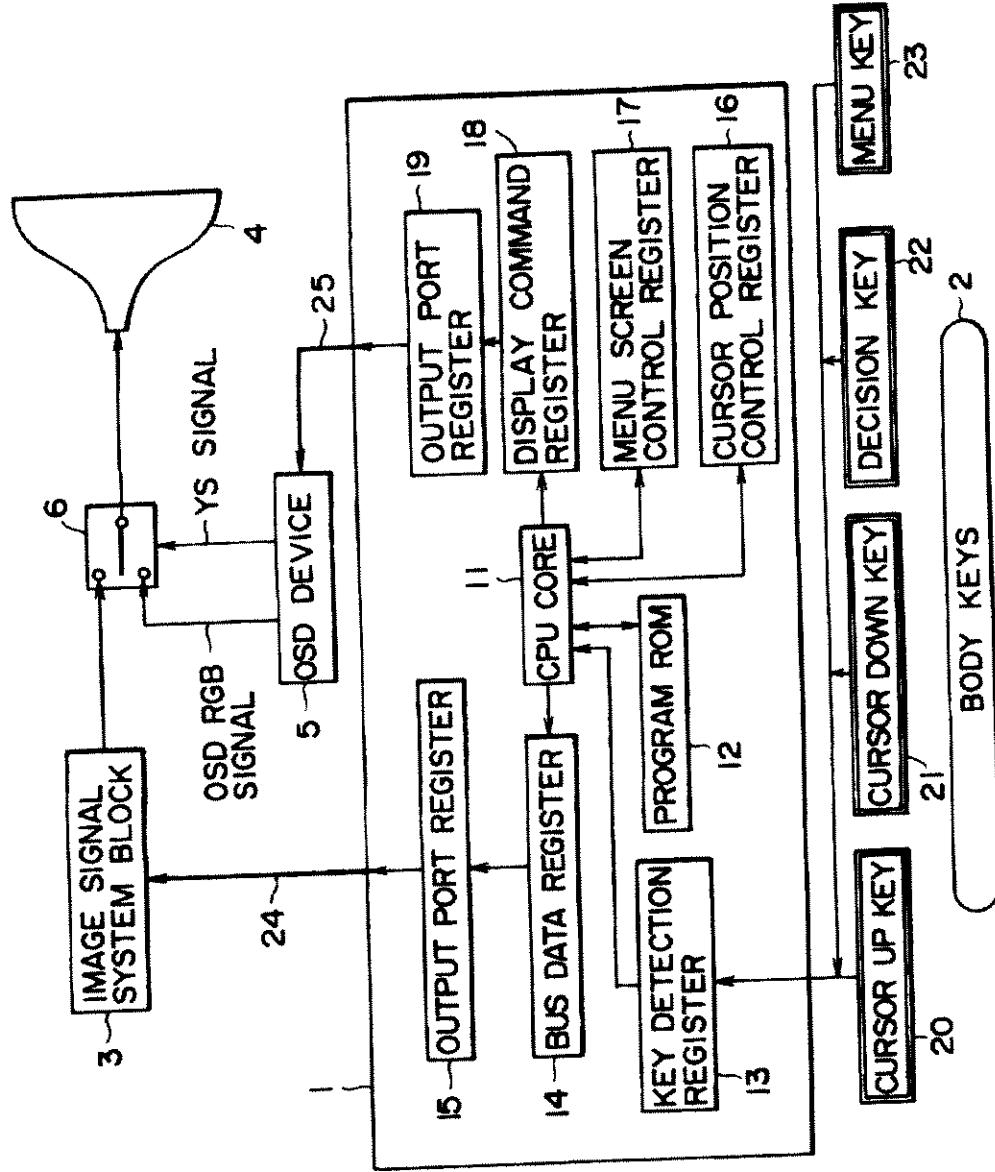


FIG. 2A

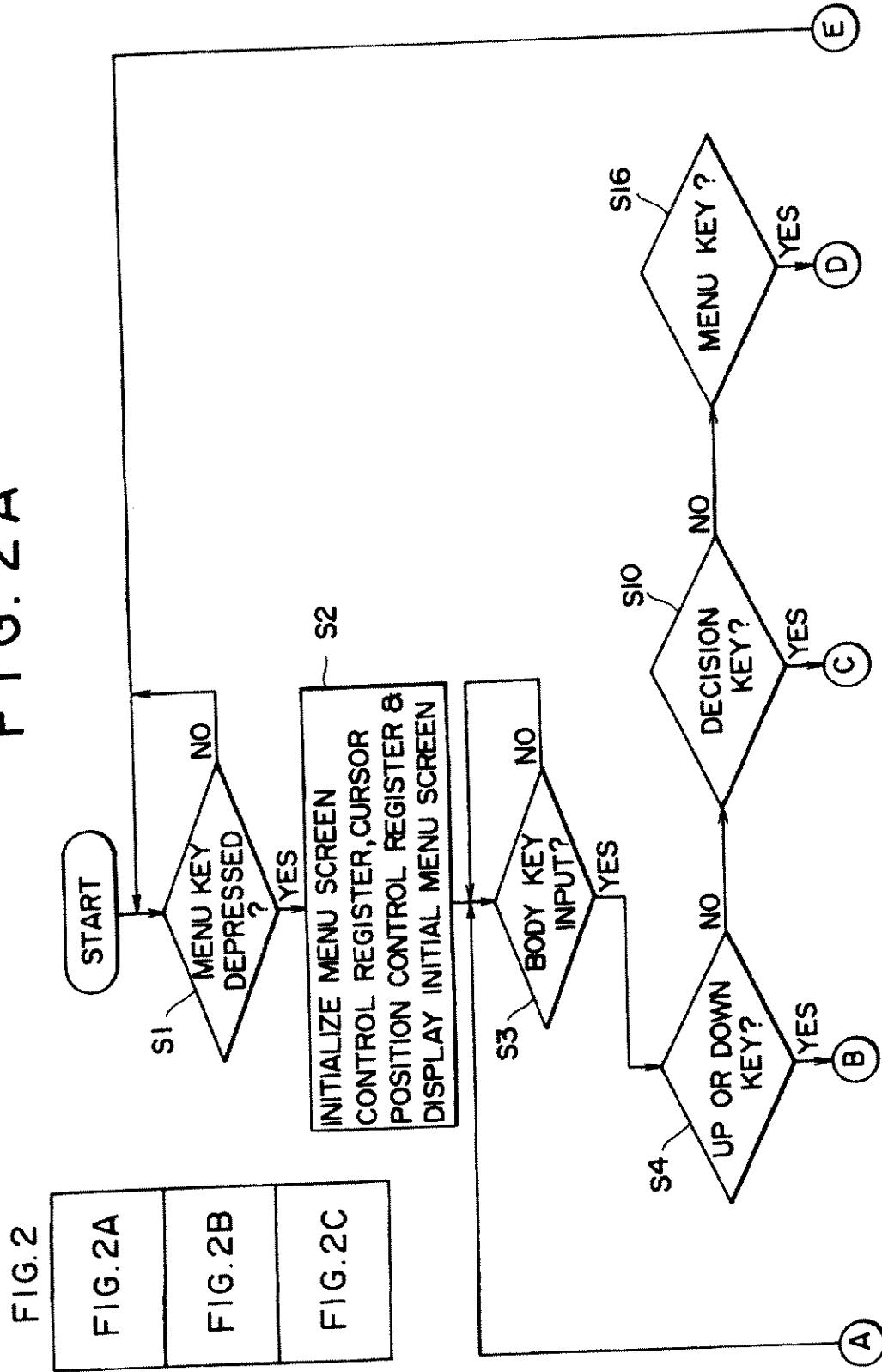


FIG. 2C

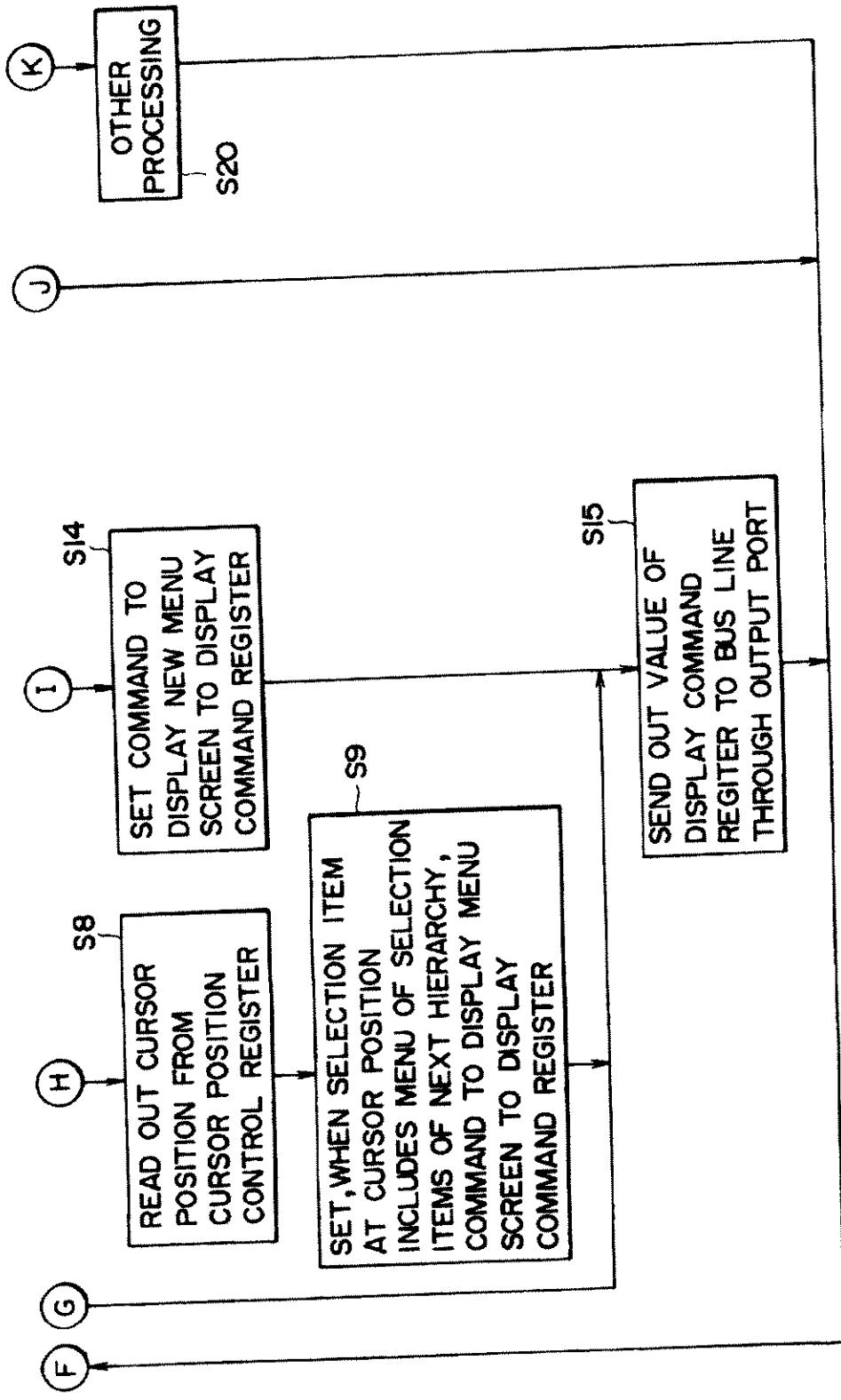


FIG. 2C

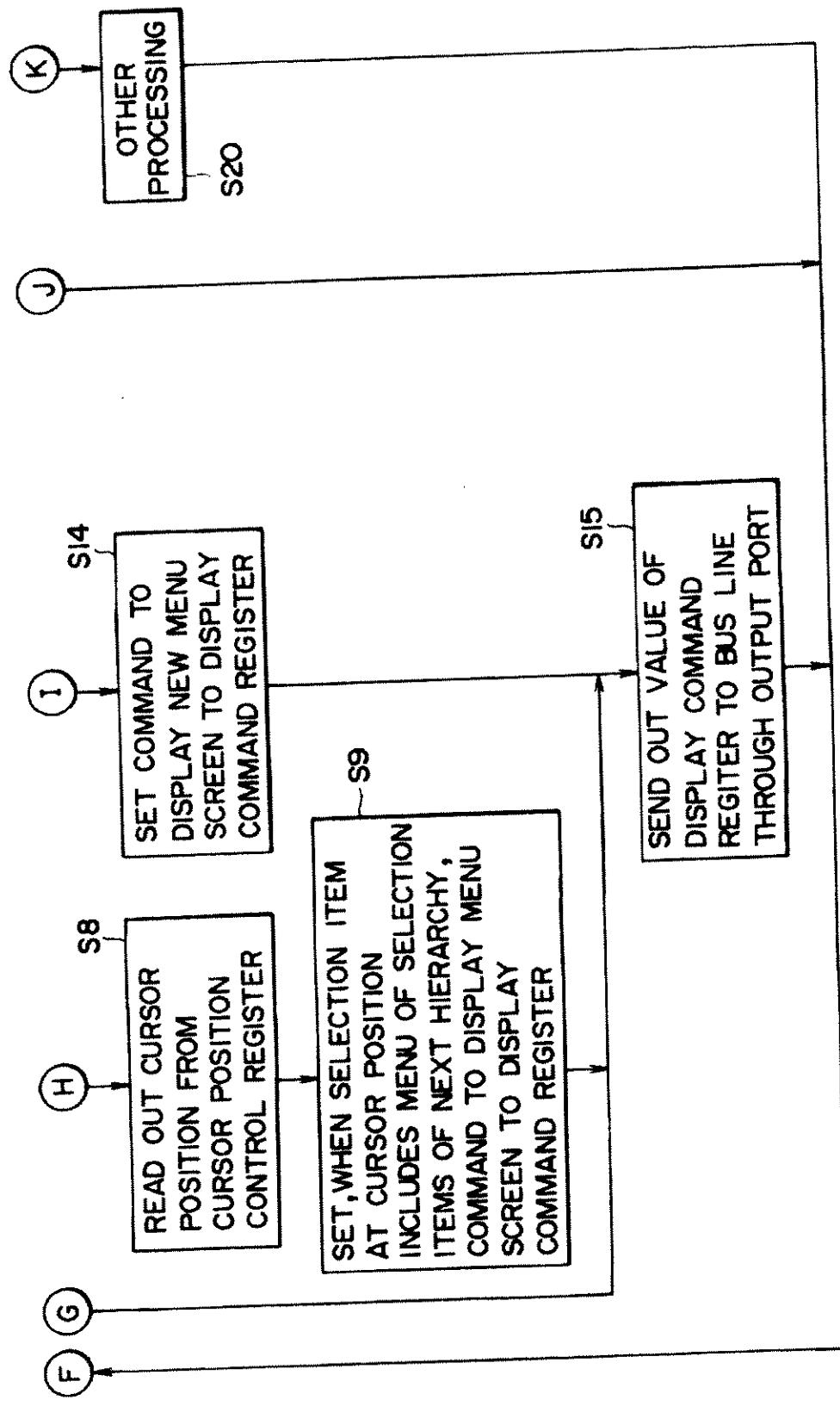
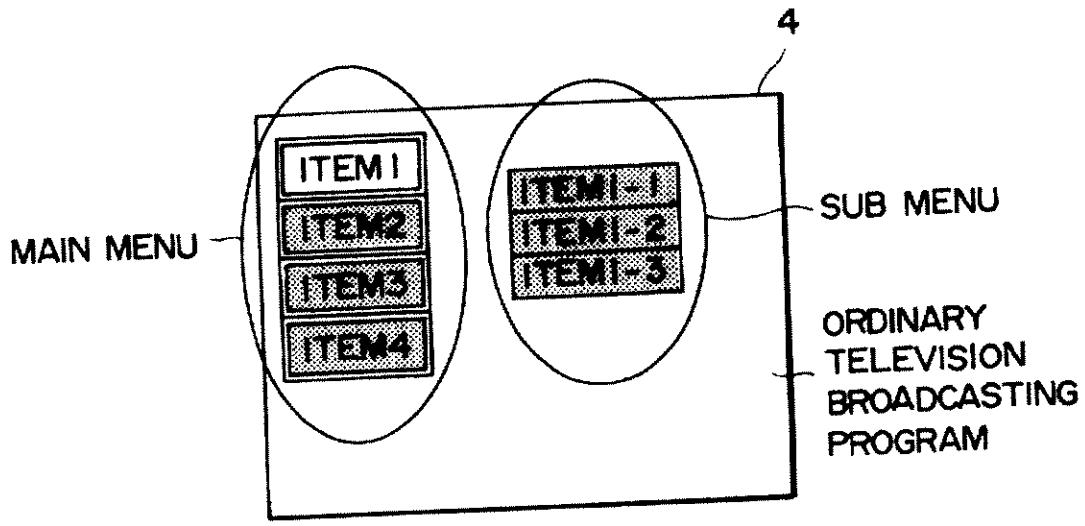
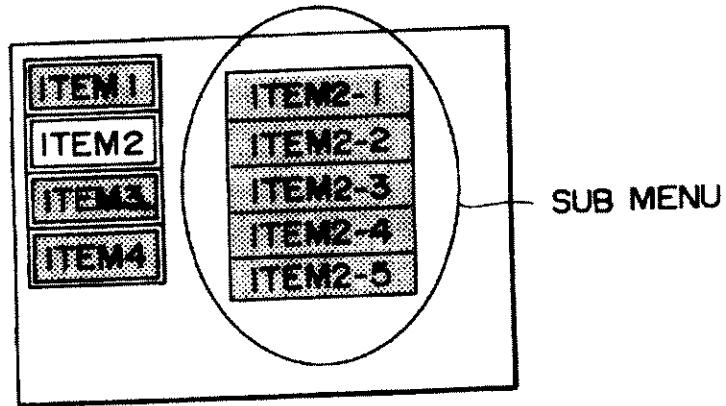


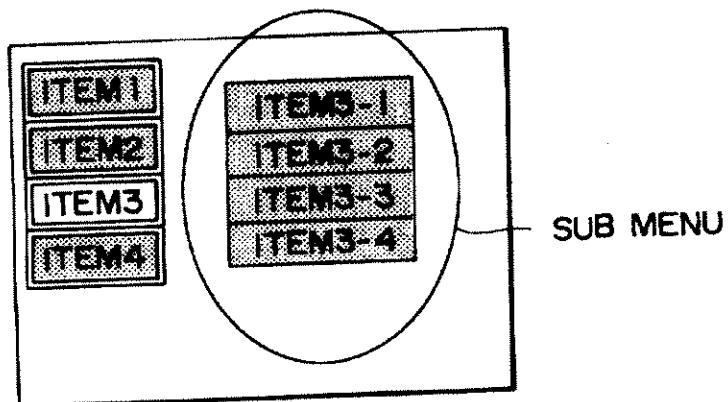
FIG. 3



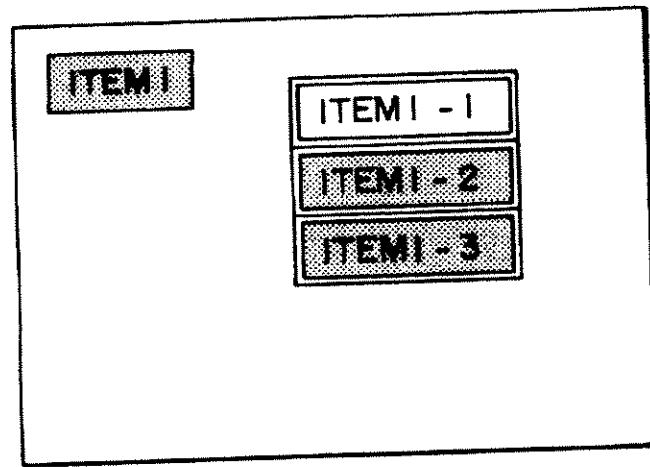
F I G. 4A



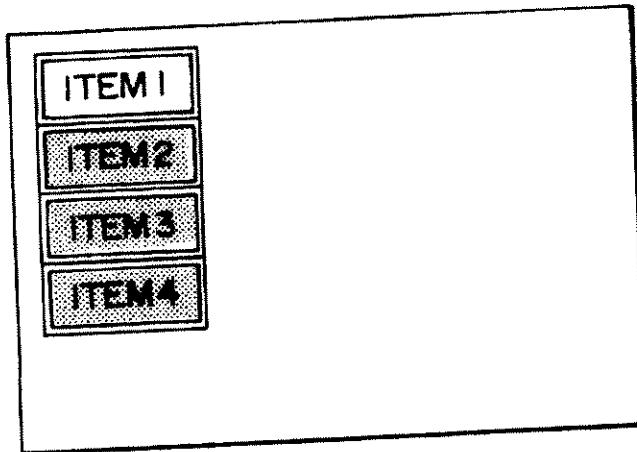
F I G. 4B



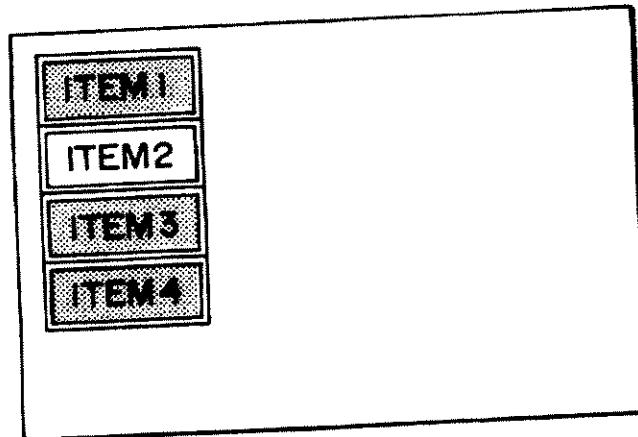
F I G. 5



F I G. 6A



F I G. 6B



F I G. 6C

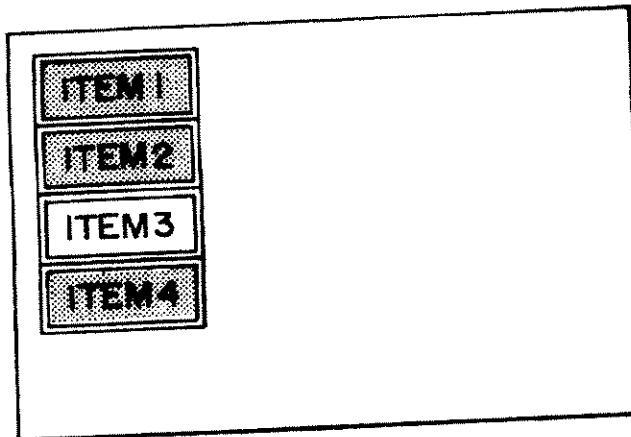


FIG. 7

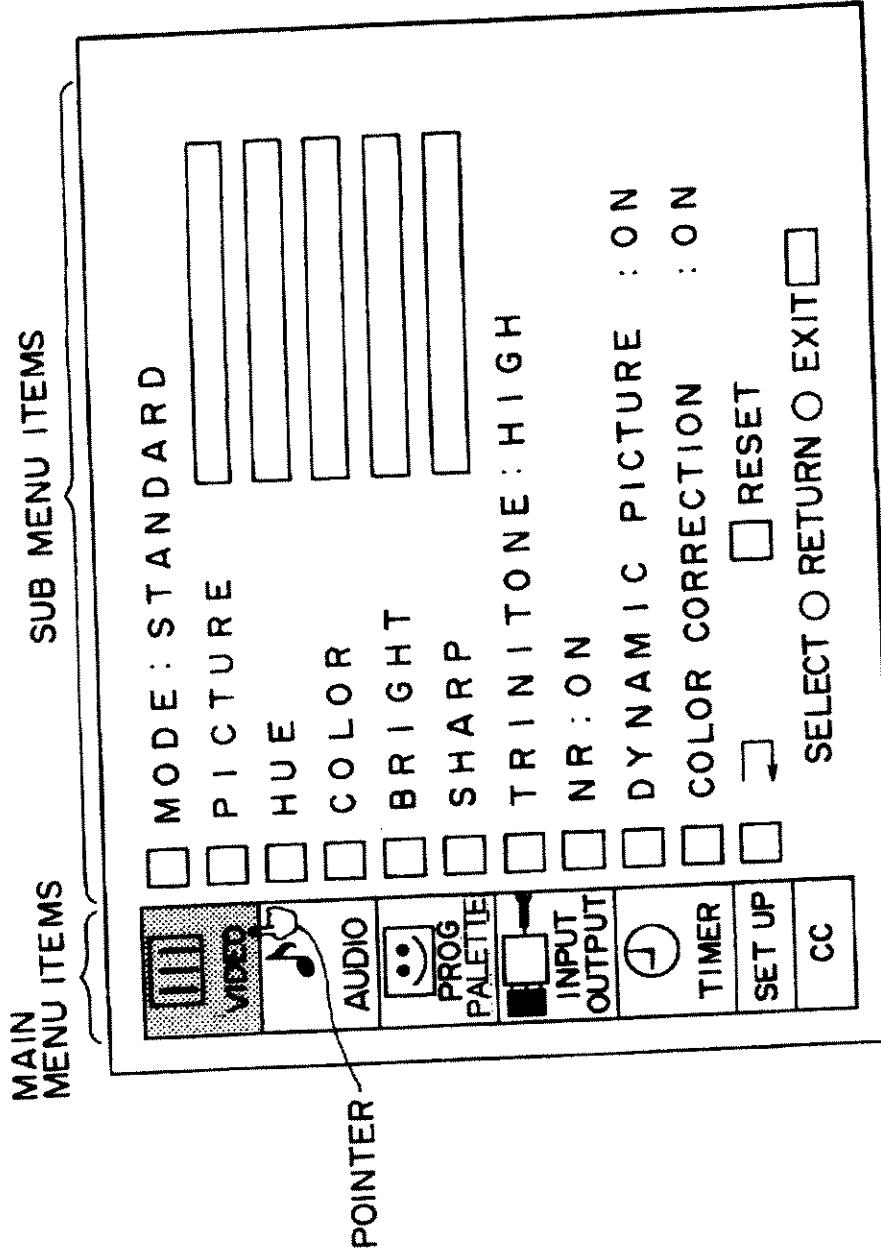


FIG. 8

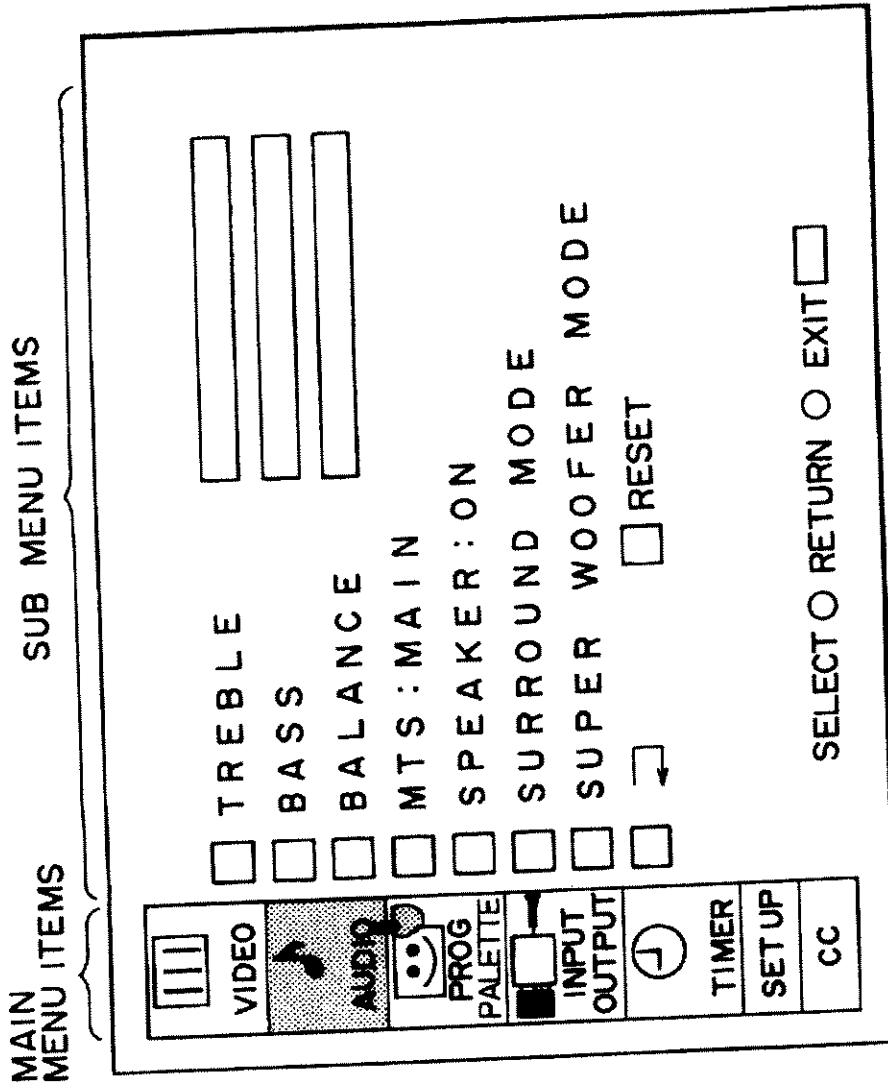


FIG. 9

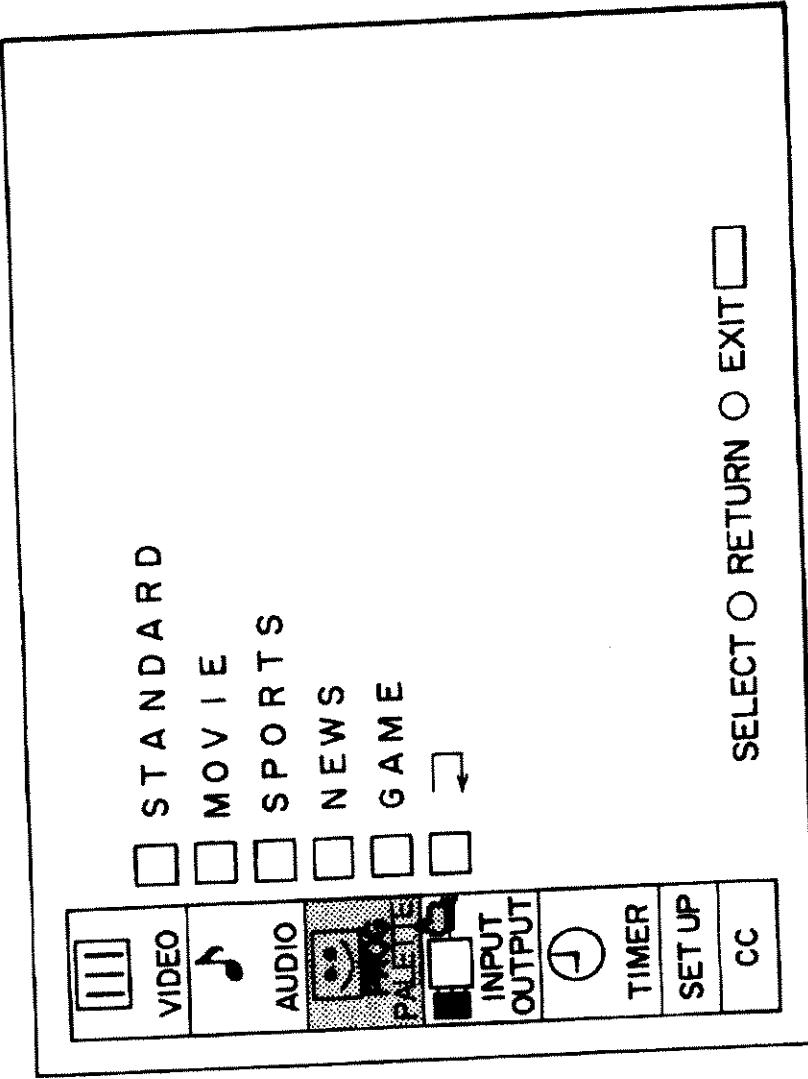


FIG. 10

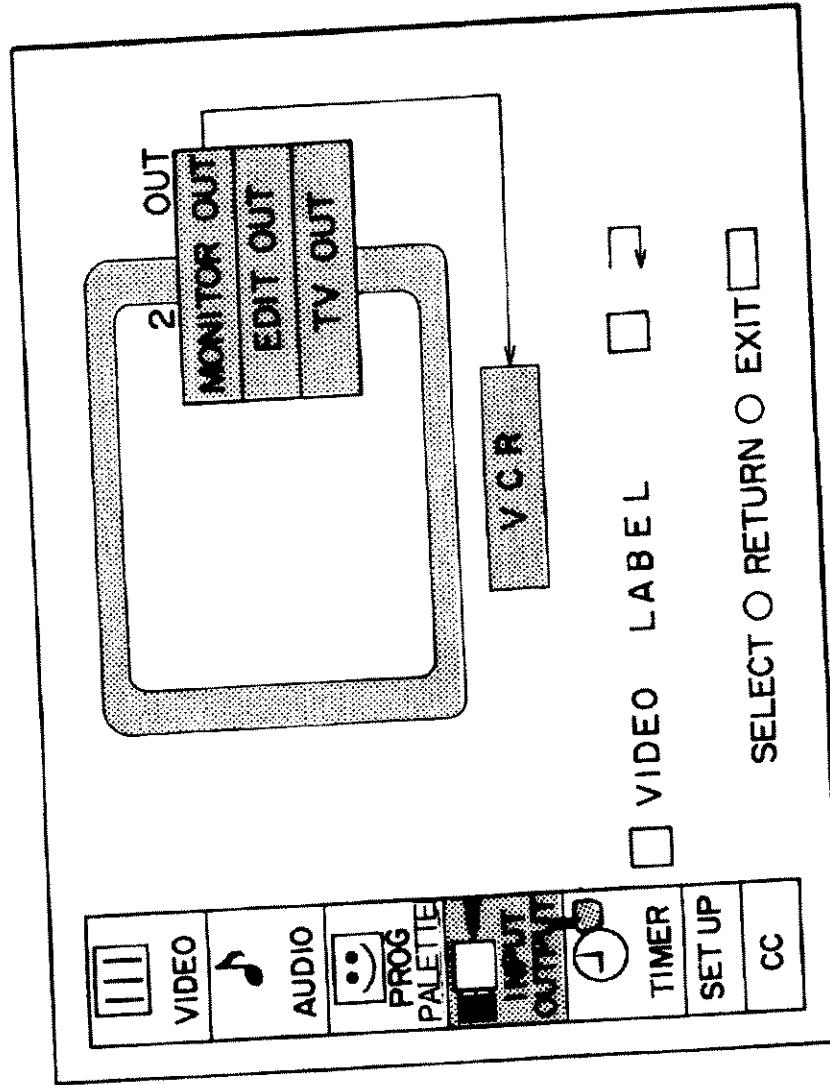


FIG. II

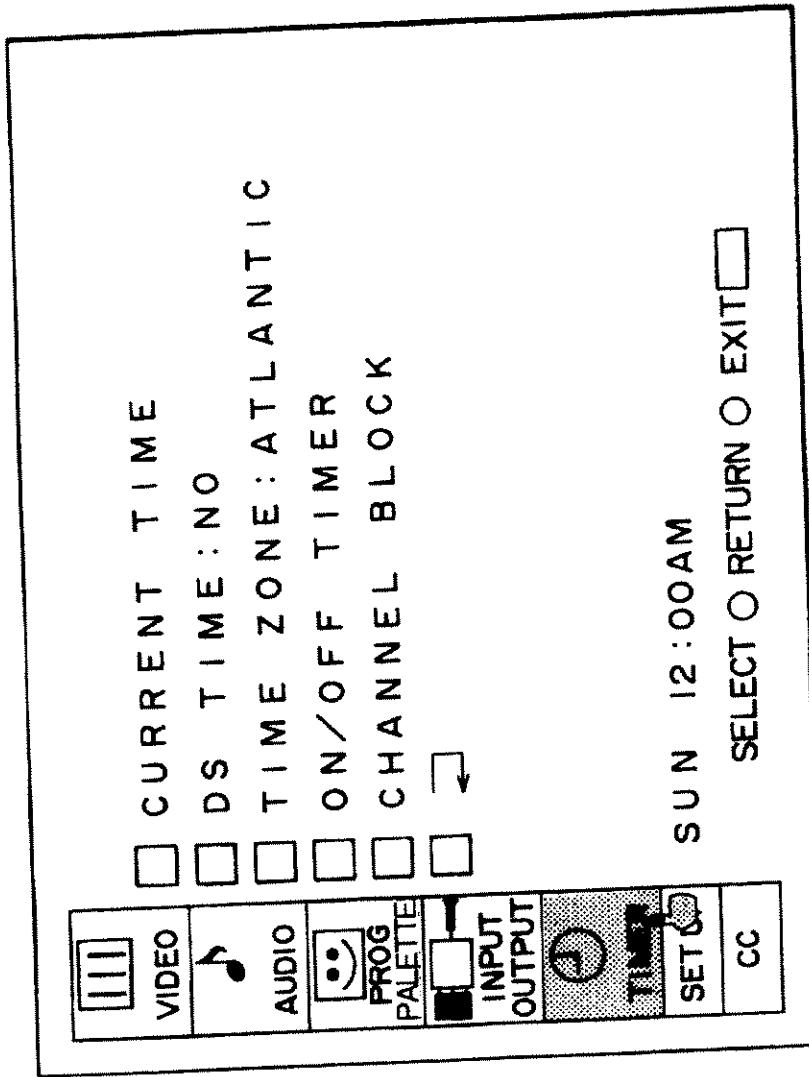


FIG. 12

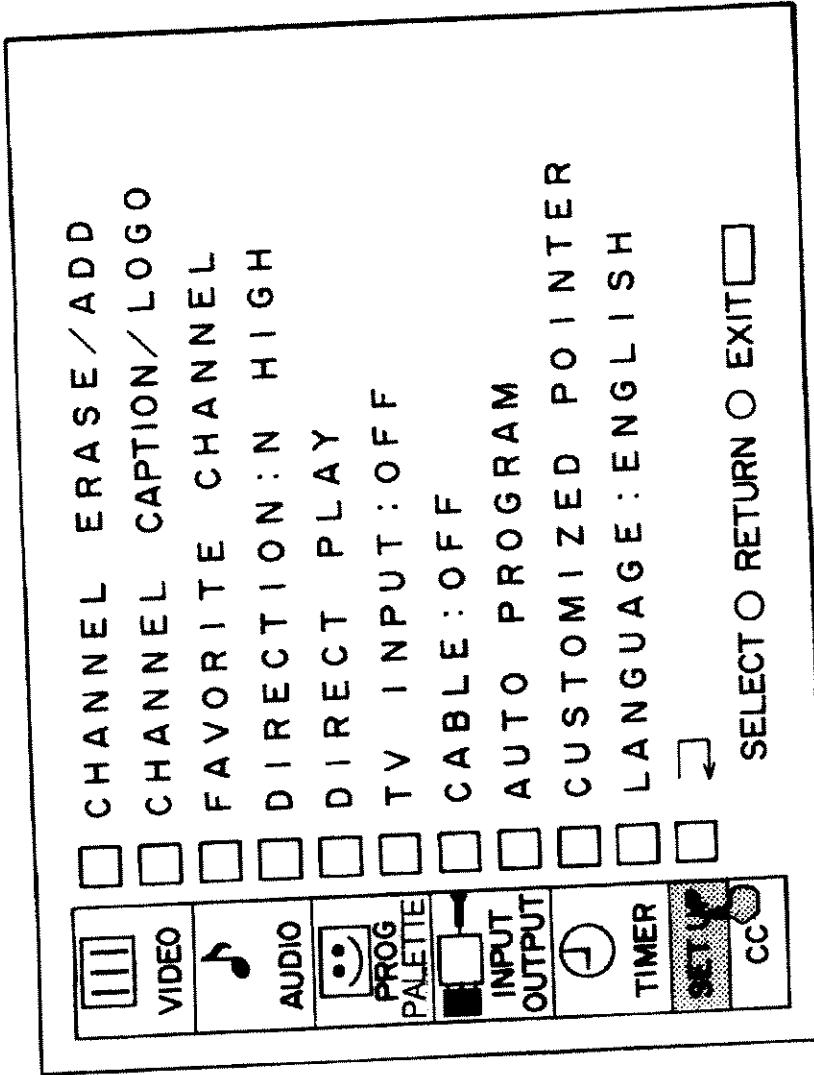


FIG. 13

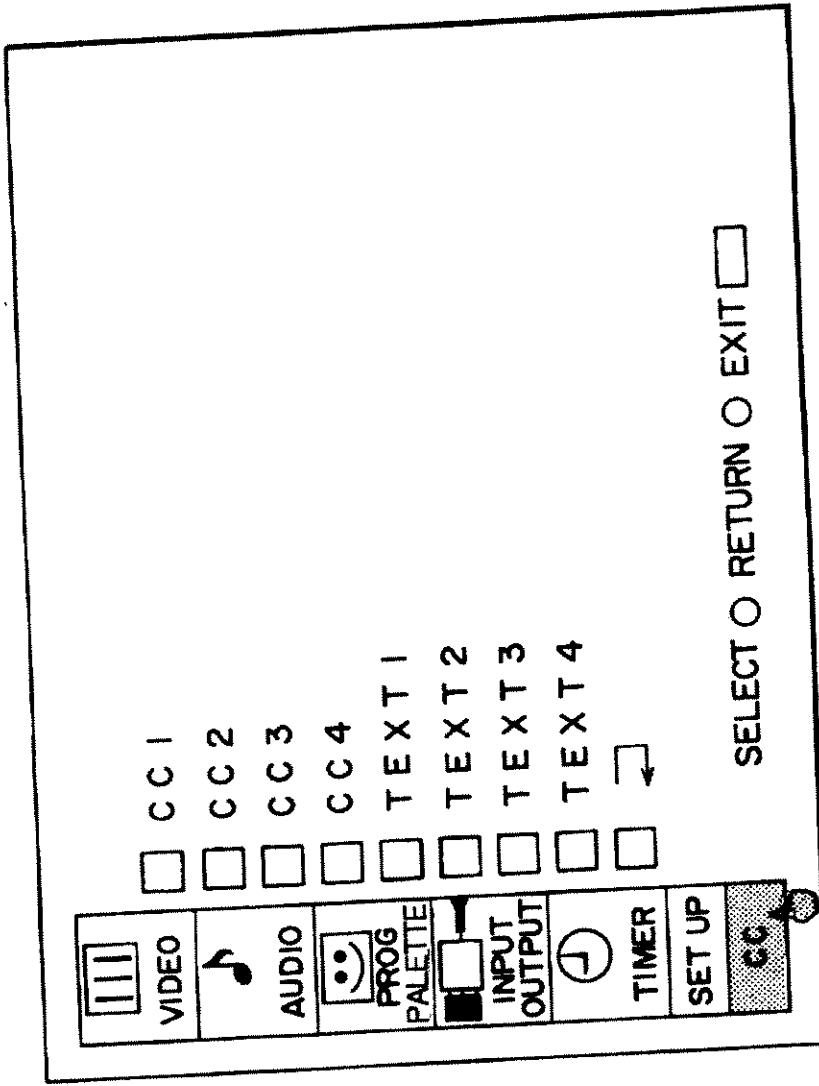


FIG. 14

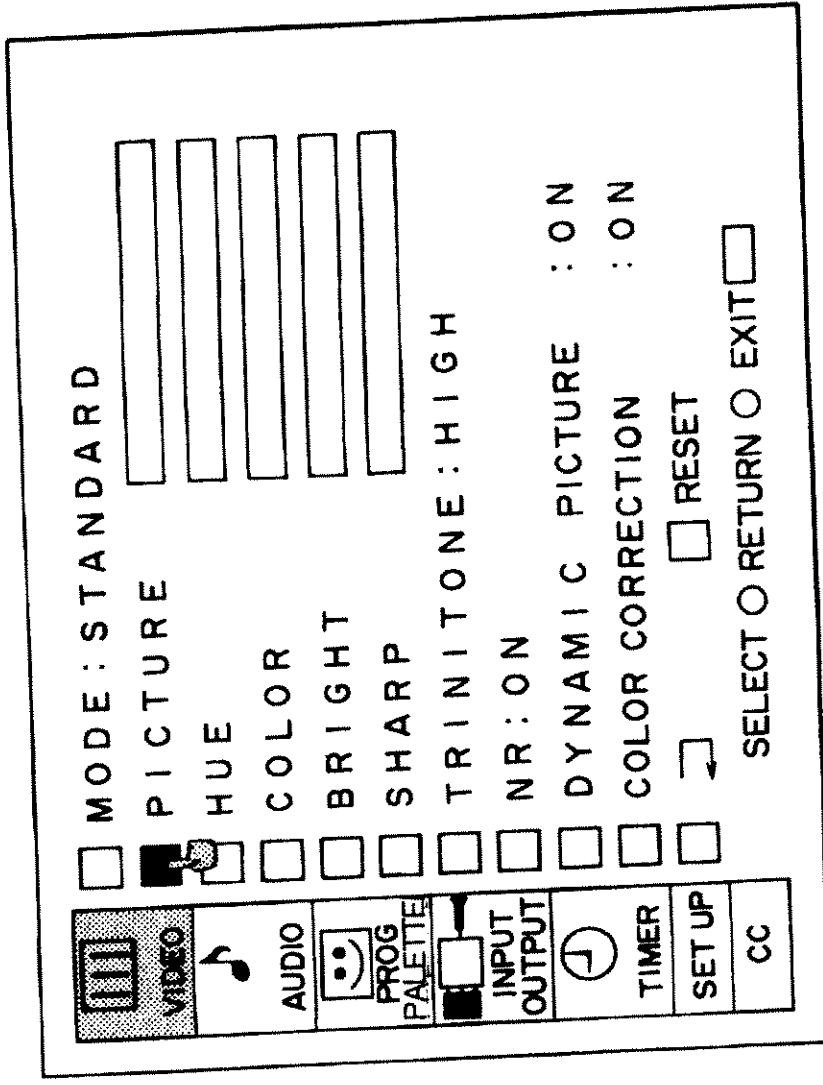


FIG. 15

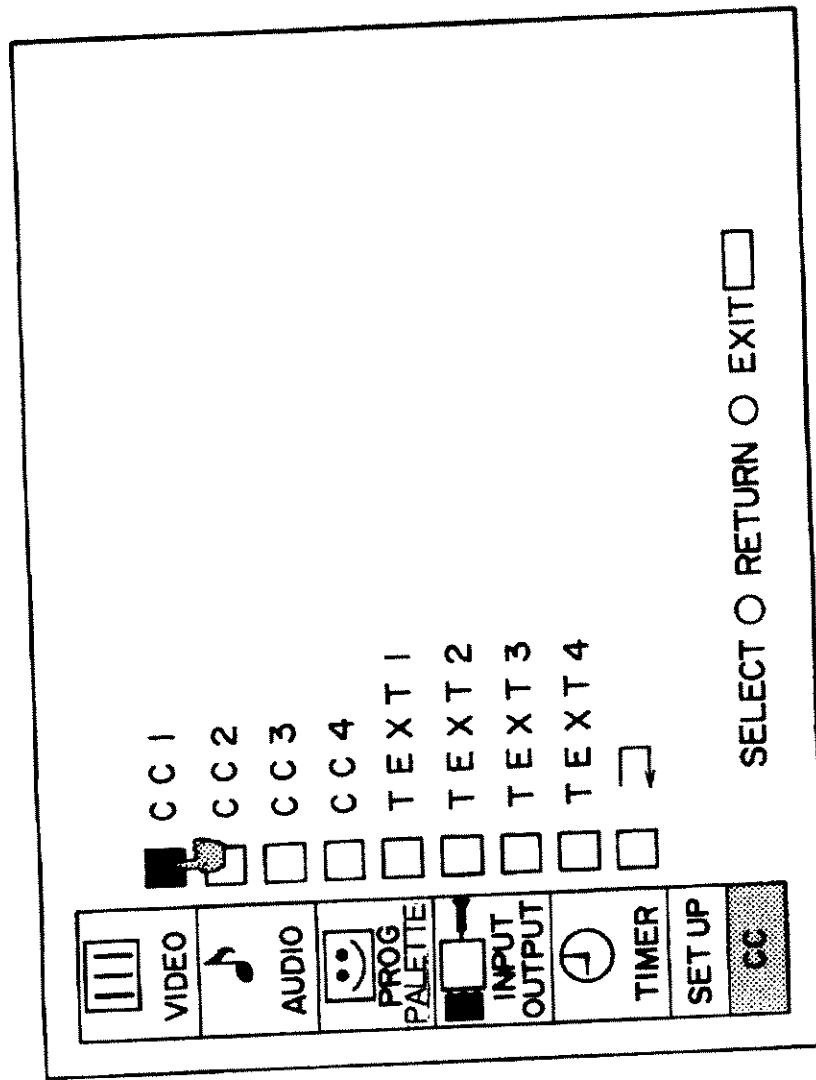


FIG. 16

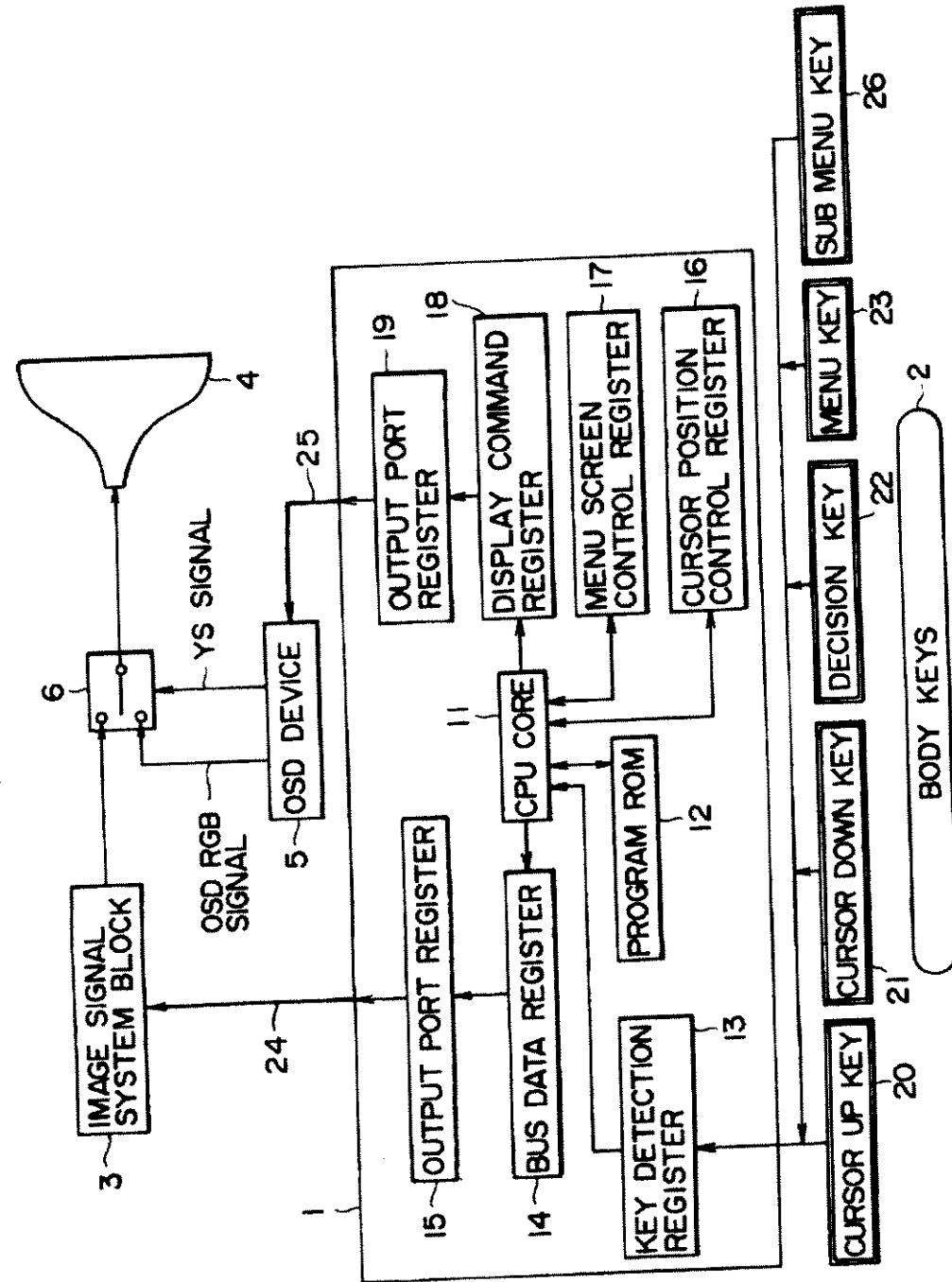


FIG. 17

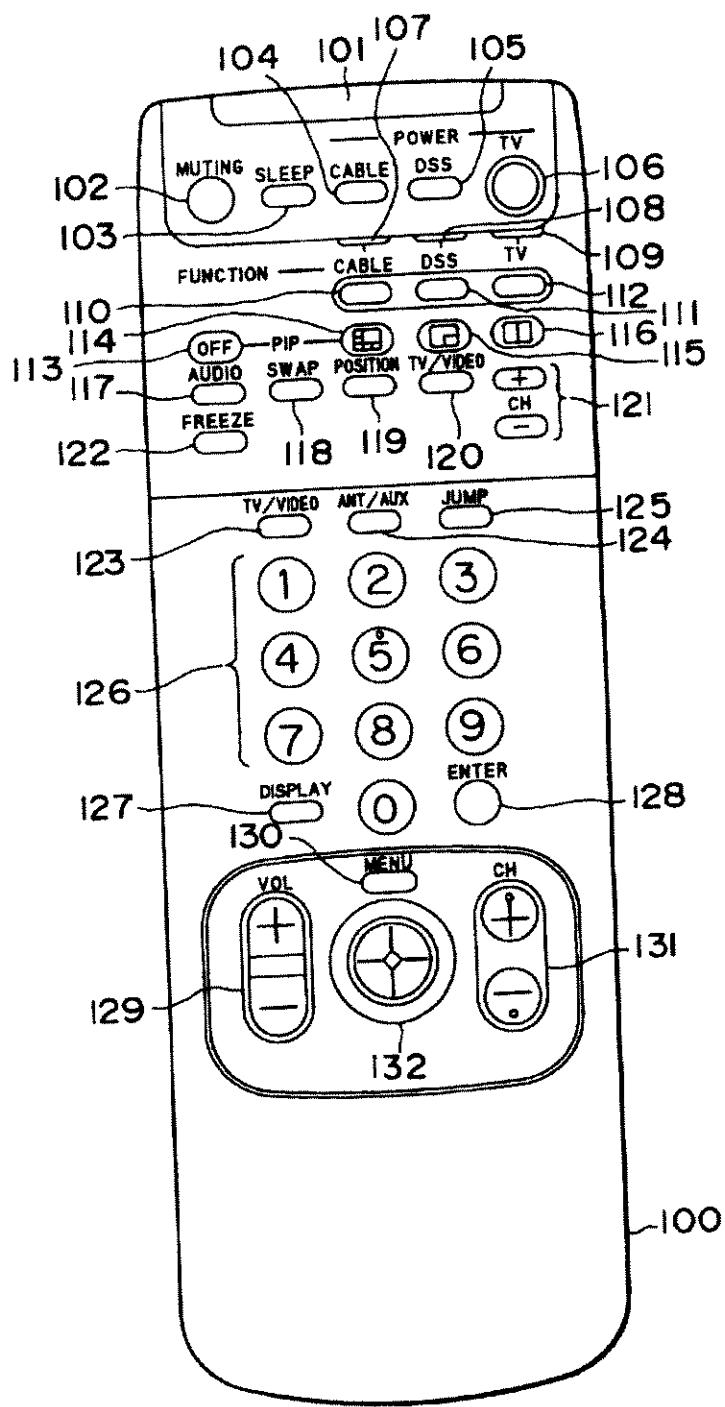


FIG. 18

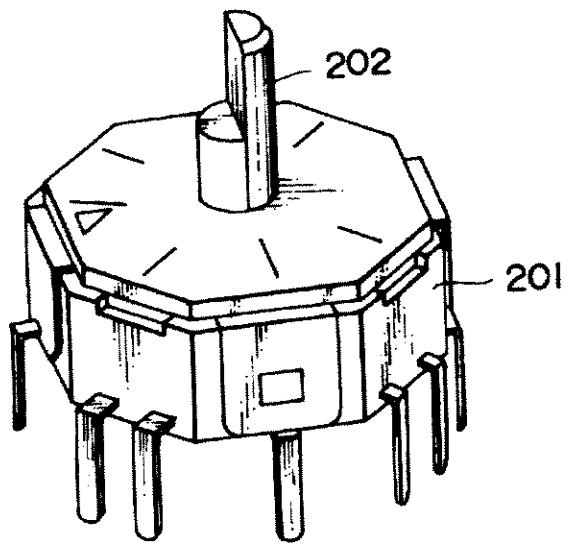


FIG. 19

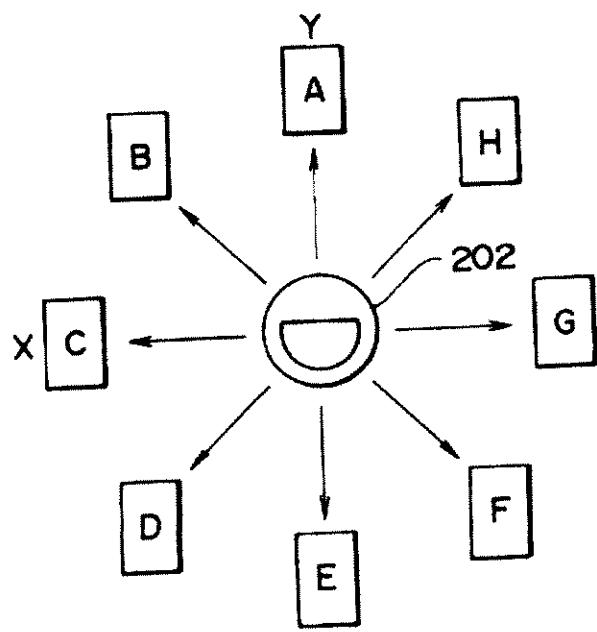


FIG. 20

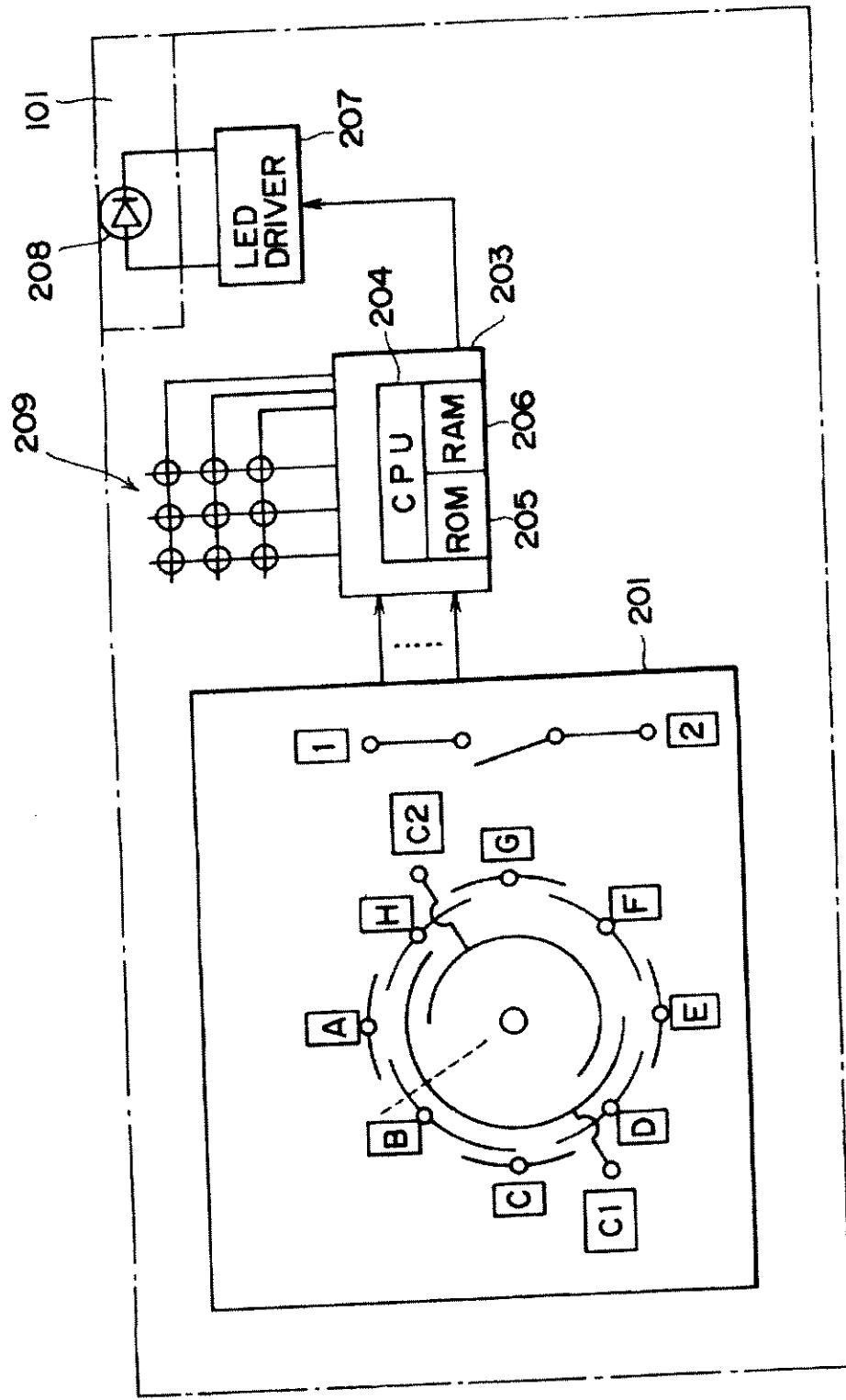
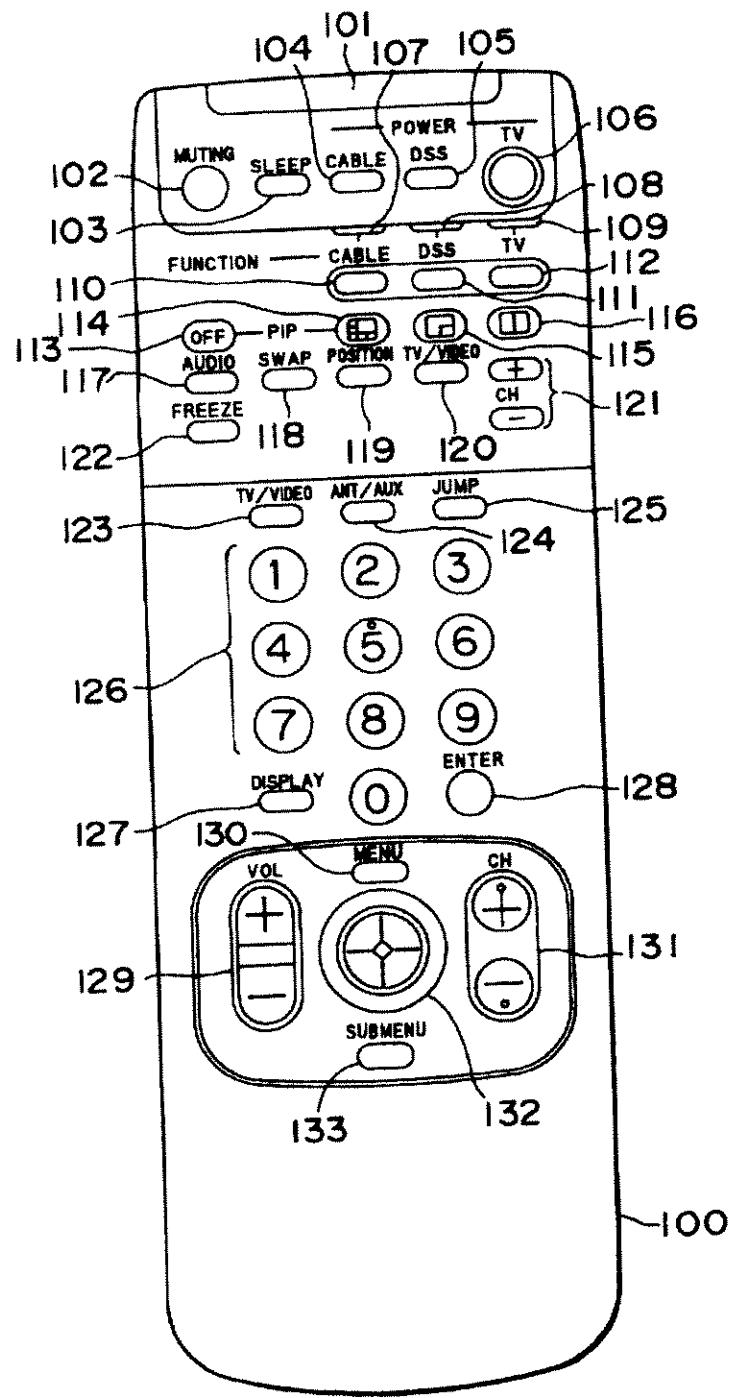


FIG. 21



**TELEVISION FUNCTION SELECTION
METHOD, TELEVISION RECEIVER AND
REMOTE COMMANDER FOR TELEVISION
RECEIVER**

BACKGROUND OF THE INVENTION

This invention relates to a television function selection method, a television receiver and a remote commander for a television receiver, and more particularly to a television function selection method, a television receiver and a remote commander for a television receiver wherein, for example, a hierarchical menu is displayed on a screen of the television receiver and a predetermined function is selected from a displayed menu.

Conventionally, in order to select a function of a television receiver, a user first manually operates an operation panel of a television receiver or a remote commander for the television receiver to display a menu corresponding to the highest level of hierarchy on the screen of the television receiver. The menu is formed of a plurality of selection items or alternatives corresponding to functions of the television receiver.

Then, the user manually operates the operation panel or the remote commander to select one of the selection items. When the selected selection item has selection items of a lower hierarchy relating thereto, the menu of the highest hierarchy level is erased, and the menu of the lower hierarchy is displayed on the screen instead. Then, the user selects one of selection items forming the menu of the lower hierarchy which corresponds to a predetermined function. Consequently, a desired function can be selected. Thereafter, the television receiver performs a predetermined operation based on the selected function.

However, in the case where a function of a television receiver is selected in such a manner as described above, when a menu of a lower hierarchy is displayed, since a menu of a hierarchy at the higher position in the hierarchical structure than the lower hierarchy is erased, it is difficult to understand the relationship between the upper hierarchy and the lower hierarchy. Accordingly, it sometimes occurs that, before a selection item desired to be selected finally is displayed and selected, changing over between hierarchies must be repeated several times. Therefore, the conventional selection of a function of a television receiver is disadvantageous in that complicated cumbersome operations are required.

Further, when it is attempted to select a predetermined selection item from among selection items forming a menu of an upper hierarchy, since selection items of a menu of a lower hierarchy relating to the predetermined selection item cannot be displayed prior to the selection, it is difficult to recognize the structure of the hierarchical menu. Consequently, the conventional selection of a function of a television receiver is disadvantageous also in that even a user who understands a menu structure to some degree must recall the menu structure to mind every time. Operations are difficult for ordinary users.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a television function selection method, a television receiver and a remote commander for a television receiver wherein a function of a television receiver can be selected simply and rapidly.

In order to attain the object described above, according to an aspect of the present invention, there is provided a

television function selection method, comprising the steps of displaying, in a first region of a screen of a television receiver, selection items of one of hierarchies of a hierarchical menu which includes a plurality of hierarchies each including selection items corresponding to functions of the television receiver, designating one of the selection items of the first hierarchy of the menu displayed on the screen of the television receiver, displaying, while the selection items of the first hierarchy of the menu are displayed in the first region of the screen, a lower menu which is a lower hierarchy to the first hierarchy of the menu displayed and includes relating selection items relating to the designated selection item in a second region of the screen of the television receiver which is outside the first region or outside at least a portion of the first region, selecting the designated selection item of the first hierarchy, and selecting one of the related selection items relating to the selected selection item of the first hierarchy.

In the television function selection method, if one of the selection items of a menu displayed in the first region of the screen is designated, then while the menu remains displayed on the screen of the television receiver, a lower menu which is subordinate to the hierarchy of the menu displayed and includes relating selection items relating to the designated selection item is displayed in the second region of the screen different from the first region. Consequently, menus of a plurality of hierarchies can be displayed simultaneously on the screen of the television receiver. Accordingly, the menu structure can be grasped simply by the user, and a desired function of the television receiver can be selected simply and rapidly without the necessity of performing an unnecessary operation.

The number of the hierarchies of the menu may be equal to or greater than 2.

According to another aspect of the present invention, there is provided a television function selection method, comprising the steps of displaying, in a first region of a screen of a television receiver, selection items of one of hierarchies of a hierarchical menu which includes a plurality of hierarchies each including selection items corresponding to functions of the television receiver, designating one of the selection items of the first hierarchy of the menu displayed on the screen of the television receiver, selecting the designated selection item, displaying, while the selection items of the first hierarchy of the menu or at least the selected selection item is displayed in the first region of the screen, a lower menu which is so subordinate to the first hierarchy of the menu and includes relating selection items relating to the selected selection item in a second region of the screen of the television receiver which is outside the first region or outside at least a portion of the first region, and selecting one of the relating selection items forming the displayed lower menu.

In the television function selection method, if one of the selection items of a menu displayed in the first region of the screen is designated and selected, then while the menu or at least the selected selection item remains displayed in the first region of the screen of the television receiver, a lower menu which is subordinate to the hierarchy of the menu and includes relating selection items relating to the selected selection item is displayed in the second region of the screen different from the first region. Consequently, menus of a plurality of hierarchies can be displayed simultaneously on the screen of the television receiver. Accordingly, the menu structure can be understood simply by the user, and a desired function of the television receiver can be selected simply and rapidly without the necessity of performing an unnecessary operation.

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The number of the hierarchies of the menu may be equal to or greater than 2.

According to a further aspect of the present invention, there is provided a television receiver, comprising a menu display means for displaying, in a first region of a screen of the television receiver, selection items of one of hierarchies of a hierarchical menu which includes a plurality of hierarchies each including selection items corresponding to functions of the television receiver, a designation means for designating one of the selection items of the first hierarchy of the menu displayed by the menu display means, a lower menu display means for displaying, while the selection items of the first hierarchy of the menu are displayed in the first region of the screen by the menu display means, a lower menu which is subordinate to the first hierarchy of the menu and includes relating selection items relating to the selection item designated by the designation means in a second region of the screen of the television receiver which is outside the first region or outside at least a portion of the first region, a first selection means for selecting the selection item designated by the designation means, and a second selection means for selecting one of the relating selection items relating to the selection item selected by the first selection means.

In the television receiver, if one of the selection items of a menu displayed in the first region of the screen is designated by the designation means, then while the menu remains displayed in the first region of the screen of the television receiver, a lower menu includes relating selection items relating to the designated selection item is displayed in the second region of the screen different from the first region by the lower menu display means. Consequently, menus of a plurality of hierarchies can be displayed simultaneously on the screen of the television receiver. Accordingly, the menu structure can be understood simply by the user, and a desired function of the television receiver can be selected simply and rapidly without the necessity of performing a unnecessary operation.

The number of the hierarchies of the menu may be equal to or greater than 2.

Preferably, the television receiver further comprises a setting means for setting, when one of the selection items of the one hierarchy of the menu displayed by the menu display means is designated by the designation means, whether or not a lower menu which is subordinate to the first hierarchy of the menu should be displayed on the screen, and when the setting means indicates that the lower menu should not be displayed on the screen, the lower menu display means does not display the lower menu on the screen.

In the television receiver, when one of the selection items of a menu displayed on the screen is designated by the designation means, it is set by the setting means whether or not a lower menu corresponding to the designated selection item should be displayed on the screen. Consequently, by setting so that the lower menu should not be displayed on the screen, a function of the television receiver can be selected without disturbing enjoyment of a program of a television broadcast as far as possible.

According to a still further aspect of the present invention, there is provided a remote commander for a television receiver which causes the television receiver to display on a screen of the television receiver a menu including selection items corresponding to functions of the television receiver and instructs, in response to selection of one of the selection items of the menu displayed on the screen of the television receiver, the television receiver to execute a corresponding

one of the functions. the remote commander comprising a menu display instruction means for inputting an instruction for displaying, in a first region of a screen of the television receiver, selection items of one of hierarchies of a hierarchical menu which includes a plurality of hierarchies each including selection items corresponding to functions of the television receiver, a designation means for designating one of the selection items of the first hierarchy of the menu displayed on the screen of the television receiver in response to the instruction of the menu display instruction means, a lower menu display instruction means for inputting, while the selection items of the first hierarchy of the menu are displayed in the first region of the screen in response to the instruction of the menu display instruction means, an instruction whether or not a lower menu which is subordinate to the first hierarchy of the menu and includes relating selection items relating to the selection item designated by the designation means should be displayed in a second region of the screen of the television receiver which is outside the first region or outside at least a portion of the first region, a first selection means for selecting the selection item designated by the designation means, and a second selection means for selecting one of the relating selection items relating to the selection item selected by the first selection means.

In the remote commander for a television receiver, one of the selection items of a menu displayed in the first region of the screen is designated by the designation means, and then, while the menu remains displayed in the first region of the screen of the television receiver, it is designated by the lower menu display designation means whether or not a lower menu which includes relating selection items relating to the selection item designated by the designation means should be displayed in the second region of the screen different from the first region. Consequently, menus of a plurality of hierarchies can be displayed simultaneously on the screen of the television receiver. Accordingly, the menu structure can be understood simply by the user, and a desired function of the television receiver can be selected simply and rapidly without the necessity of performing an unnecessary operation.

The number of the hierarchies of the menu may be equal to or greater than 2.

The above and other objects, features and advantages of the present invention will become apparent from the following description and the appended claims, taken in conjunction with the accompanying drawings in which like parts or elements are denoted by like reference characters.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing a construction of a television receiver to which the present invention is applied;

FIG. 2 shows a block diagram of FIGS. 2A-2C.

FIGS. 2A-2C are flow charts illustrating operation of the television receiver of FIG. 1;

FIG. 3 is a schematic view showing an example of a menu screen when an item "ITEM 1" of a main menu is designated;

FIGS. 4A and 4B are schematic views showing an example of menu screens when items "ITEM 1" and "ITEM 2" of the main menu are designated, respectively;

FIG. 5 is a schematic view showing an example of a menu screen when an item "ITEM 1-1" of a sub menu is designated;

FIGS. 6A, 6B and 6C are schematic views showing examples of a menu screen when the display of the sub menu is erased;

FIG. 7 is a schematic view showing an example of a menu screen when an item "VIDEO" of the main menu is designated;

FIG. 8 is a schematic view showing an example of a menu screen when an item "AUDIO" of the main menu is designated;

FIG. 9 is a schematic view showing an example of a menu screen when an item "PROG PALETTE" of the main menu is designated;

FIG. 10 is a schematic view showing an example of a menu screen when an item "INPUT OUTPUT" of the main menu is designated;

FIG. 11 is a schematic view showing an example of a menu screen when an item "TIMER" of the main menu is designated;

FIG. 12 is a schematic view showing an example of a menu screen when an item "SETUP" of the main menu is designated;

FIG. 13 is a schematic view showing an example of a menu screen when an item "CC" of the main menu is designated;

FIG. 14 is a schematic view showing an example of a menu screen when an item "PICTURE" of the item "VIDEO" of the main menu is designated;

FIG. 15 is a schematic view showing an example of a menu screen when an item "CC1" of the item "CC" of the main menu is designated;

FIG. 16 is a block diagram showing a construction of another television receiver to which the present invention is applied;

FIG. 17 is a schematic view showing an arrangement of buttons of a remote commander to which the present invention is applied;

FIG. 18 is a perspective view showing a structure of a select button switch of the remote commander of FIG. 17;

FIG. 19 is a diagrammatic view showing directions in which the select button switch of FIG. 18 can be moved;

FIG. 20 is a block diagram showing an internal construction of the remote commander of FIG. 17; and

FIG. 21 is a schematic view showing an arrangement of buttons of another remote commander to which the present invention is applied.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring first to FIG. 1, there is shown in block diagram a construction of a television receiver to which the present invention is applied. The television receiver includes a body key apparatus 2 (setting means) which in turn includes a cursor up (Cursor UP) key 20 (designation means), a cursor down (Cursor DOWN) key 21 (designation means), a decision key 22 (first selection means, second selection means) and a menu (Menu) key 23. If one of the keys of the body key apparatus 2 is selectively depressed, then a signal corresponding to a key code of the depressed key is supplied to a system control microcomputer (system controlling microcomputer) 1.

The system control microcomputer 1 includes a program ROM (Read Only Memory) 12 in which a predetermined program and various data are stored, a CPU (Central Processor Unit) core 11 for controlling components of the system control microcomputer 1 in accordance with the program stored in the program ROM 12, a key detection register 13 for receiving and holding a signal corresponding

to a key code supplied from the body key apparatus 2, a bus data register 14 for storing and outputting predetermined data supplied from the CPU core 11, an output port register 15 for receiving output data from the bus data register 14 and outputting the received data to an bus line 24, a cursor position control register 16 for holding data for controlling the position of a cursor, a menu screen controlling register 17 for holding data for controlling a menu screen, a display command register 18 for holding a display command for displaying a menu, and an output port register 19 for receiving an output signal corresponding to a predetermined command from the display command register 18 and outputting the received signal to another bus line 25. The system control microcomputer 1 controls a video signal system block 3 and an On Screen Display (OSD) device 5 (menu display means, lower menu display means) which will be described below.

The video signal system block 3 is controlled by a control signal supplied thereto from the output port register 15 of the system control microcomputer 1 via the bus line 24 and outputs a predetermined video signal.

The OSD device 5 generates, in accordance with a control signal supplied thereto from the system control microcomputer 1 via the bus line 25, an RGB signal of OSD data corresponding to a character, a graphic form, a cursor or the like for displaying a predetermined menu screen and a control signal (YS signal) for controlling a switch 6. The generated signals are supplied to the switch 6.

The switch 6 is controlled by the CPU core 11 and changes over the internal connection thereof so that it selectively receives one of a video signal supplied from the video signal system block 3 or an RGB signal supplied from the OSD device 5 corresponding to OSD data and supplies the selected signal to a CRT 4.

The CRT 4 displays, on the screen thereof, an image corresponding to a video signal supplied thereto from the switch 6 or a character, a graphic form or the like corresponding to an RGB signal of OSD data.

Operation of the television receiver described above will be described subsequently with reference to the flow charts of FIGS. 2A-2C. First at step S1, it is discriminated whether or not the menu key 23 of the body key apparatus 2 provided on the body of the television receiver is depressed by a user. In the discrimination, the CPU core 11 reads out data stored in the key detection register 13 and discriminates whether or not the data is key code data corresponding to the menu key 23.

When the CPU core 11 discriminates that the menu key 23 is not depressed, the processing at step S1 is executed repetitively. On the other hand, when it is discriminated that the menu key 23 is depressed, the control sequence advances to step S2.

At step S2, initial values are placed into the menu screen controlling register 17 and the cursor position control register 16. In particular, information representing that, for example, the highest hierarchy level of a hierarchical menu is an object of control at present is placed into the menu screen controlling register 17, and information representing that the cursor is positioned at the first item of the menu of the highest hierarchy level is placed into the cursor position control register 16.

Then, in accordance with the information, the CPU core 11 places a predetermined display command for displaying a corresponding menu screen into the display command register 18. The display command is supplied to the OSD device 5 via the output port register 19 and the bus line 25.

The OSD device 5 generates an RGB signal of predetermined OSD data corresponding to the display command supplied thereto and supplies the RGB signal to the switch 6. The OSD device 5 further generates a control signal for changing over the internal connection of the switch 6 so that an output signal of the OSD device 5 may be supplied to the CRT 4 or so that a video signal outputted from the video signal system block 3 may be supplied to the CRT 4. The control signal thus generated is supplied to the switch 6.

In particular, where a menu is to be displayed, the internal connection of the switch 6 is changed over so that an output signal of the OSD device 5 may be supplied to the CRT 4, but where a program of an ordinary television broadcast is to be displayed, the internal construction of the switch 6 is changed over so that a video signal outputted from the video signal system block 3 may be supplied to the CRT 4.

As a result, a menu is displayed on the screen of the CRT 4 in a superposed relationship with a program of an ordinary television broadcast as shown in FIG. 3. In this instance, the main menu of the highest hierarchy level is displayed on a left side portion of the screen while a sub menu of a lower hierarchy level is displayed on a right side portion of the screen. In this instance, the main menu is formed of, for example, items "ITEM 1" to "ITEM 4" each formed with an icon, and, the first item "ITEM 1" of the main menu is displayed in such an emphasized condition that it is displayed in a reversed condition or in a highlighted condition. Then, a sub menu of the highlighted "ITEM 1" displayed is displayed on the right side portion of the screen. In this instance, "ITEM 1-1" to "ITEM 1-3" are displayed as the items of the sub menu.

Thereafter, the control sequence advances to step S3, at which it is discriminated whether or not one of the keys of the body key apparatus 2 is depressed. In this instance, the discrimination of depression of a key of the body key apparatus 2 depends upon whether or not key data corresponding to one of the keys of the body key apparatus 2 is stored in the key detection register 13. When it is discriminated that none of the keys of the body key apparatus 2 is depressed, the processing at step S3 is executed repetitively. On the other hand, if it is discriminated that one of the keys of the body key apparatus 2 is depressed, the control sequence advances to step S4.

At step S4, the key data detected by the key detection register 13 is decoded, and it is discriminated whether or not the depressed key of the body key apparatus 2 is one of the cursor up key 20 or the cursor down key 21. If it is discriminated that the depressed key of the body key apparatus 2 is one of the cursor up key 20 or the cursor down key 21, the control sequence advances to step S5. At step S5, a new position of the cursor is determined from the cursor position at present, in this instance, the position of the highlighted displayed item, the kind of the depressed key. The value of the cursor position control register 16 is re-written with the new cursor position.

Then, the control sequence advances to step S6, at which a display command for displaying the main menu in which an item corresponding to the new cursor position is displayed highlighted on the screen in order to reflect on the screen that the cursor has moved recently is placed into the display command register 18.

Then at step S7, it is discriminated whether or not the television receiver is set by a user so that a sub menu of the lower hierarchy corresponding to the item on the main menu at which the cursor is positioned is to be displayed. Up on the setting whether or not the sub menu should be displayed,

as hereinafter described in connection with step S18, a flag for setting the display of a sub menu to be displayed as an item of the main menu on the screen to on (to be displayed) or off (not to be displayed) is selected.

When it is discriminated at step S7 that the television receiver is not set so that a sub menu of the lower hierarchy corresponding to the item at which the cursor is positioned at present is displayed, the control sequence advances to step S15. At step S15, the display command placed in the display command register 18 is outputted to the bus line 25 via the output port register 19 and supplied to the OSD device 5. The OSD device 5 generates an RGB signal of OSD data and a control signal corresponding to the received display command and supplies the signals to the switch 6. The switch 6 changes over the internal connection thereof in response to the control signal supplied thereto and supplies the RGB signal of the OSD data at a predetermined timing to the CRT 4. In this instance, since it is not set by the user so as to display a sub menu, a display command for displaying a sub menu is not placed in the display command register 18, and consequently, the sub menu is not displayed while only the main menu is displayed.

On the other hand, where the television receiver is set so as to display a sub menu of the lower hierarchy, the control sequence advances to step S8, at which information corresponding to the cursor position is read out from the cursor position control register 16. Then, the control sequence advances to step S9, at which, when there is a sub menu of the lower hierarchy relating to the selection item on the main menu at which the cursor is positioned, a display command for displaying the sub menu is placed into the display command register 18, whereafter the control sequence advances to step S15.

If, for example, the cursor down key 21 is depressed by a user, then a display command for displaying a screen on which the cursor is moved to the item "ITEM 2" of the main menu is placed into the display command register 18 and supplied from the output port register 19 to the OSD device 5 via the bus line 25 under the control of the CPU core 11. The OSD device 5 generates an RGB signal of OSD data and a control signal corresponding to the menu screen on which the cursor is moved to the "ITEM 2" and supplies the signal to the switch 6.

The RGB signal supplied to the switch 6 is supplied at a predetermined timing to the CRT 4 as a result of a changing over operation of the switch 6 in accordance with the control signal. Consequently, such a menu screen as shown in FIG. 4A is displayed. In this manner, the "ITEM 2" is displayed highlighted and a sub menu corresponding to the "ITEM 2" is displayed. In this instance, the sub menu of the "ITEM 2" includes items "ITEM 2-1" to "ITEM 2-5".

Further, if the cursor down key 21 is depressed by the user, then such a menu screen as shown in FIG. 4B is displayed in a similar manner as described above. In this instance, the "ITEM 3" is displayed highlighted, and a sub menu of the "ITEM 3" is displayed. Here, the sub menu of the "ITEM 3" includes items "ITEM 3-1" to "ITEM 3-4".

On the other hand, if the selection item on the main menu at which the cursor is positioned has no sub menu of lower hierarchy relating thereto at step S9, then no processing is executed, and the control sequence advances directly to step S15. At step S15, the CPU core 11 produces a display command for displaying the cursor at the cursor position read out from the cursor position control register 16 and supplies the display command to the display command register 18. The display command is thereafter supplied to the OSD device 5 via the output port register 19 and the bus line 25.

The OSD device 5 generates an RGB signal of predetermined OSD data and a control signal in response to the display command supplied thereto and supplies the signals to the switch 6. The RGB signal supplied to the switch 6 is supplied at a predetermined timing to the CRT 4, on which a corresponding menu screen is displayed. In this instance, the predetermined item of the main menu is displayed highlighted, and no corresponding sub menu to the item is displayed since such sub menu does not exist.

If it is discriminated at step S4 that the depressed key of the body key apparatus 2 is neither the cursor up key 20 nor the cursor down key 21, the control sequence advances to step S10, at which it is discriminated whether or not the depressed key of the body key apparatus 2 is the decision key 22. When it is discriminated that the depressed key of the body key apparatus 2 is not the decision key 22 then the control sequence advances to step S16. On the other hand, if the depressed key of the body key apparatus 2 is the decision key 22, the control sequence advances to step S11.

At step S11, for example, information regarding the hierarchy of the menu which is an object of processing at present is read out from the menu screen controlling register 17 while cursor position information regarding the position of the cursor at present is read out from the cursor position control register 16 by the CPU core 11. Then, the control sequence advances to step S12, at which the item on the main menu whose selection has been indicated by the depression of the decision key 22 is recognized based on the information thus read out and it is discriminated whether or not a sub menu of lower hierarchy relating to the recognized item is present.

If it is discriminated that the predetermined item on the main menu whose selection has been indicated does not have a sub menu positioned in a lower hierarchy to it, the control sequence advances to step S18. On the other hand, if it is discriminated that a sub menu of lower hierarchy is present, then the control sequence advances to step S13. At step S13, a pointer in the program which represents the position at which the cursor is present is set to the first item of the sub menu present in the lower hierarchy to the main menu by the CPU core 11. Consequently, processing such as movement of the cursor or selection of an item is thereafter performed on that sub menu of the hierarchy.

Then, cursor position information corresponding to the position of the first item of the sub menu is written into the cursor position control register 16 so that the cursor may be displayed on the first item of the sub menu.

Thereafter, the control sequence advances to step S14, at which a display command for displaying a new menu screen is produced by the CPU core 11 and placed into the display command register 18. The display command placed in the display command register 18 is supplied, at step S15, to the OSD device 5 via the output port register 19 and the bus line 25. The OSD device 5 generates an RGB signal corresponding to the new menu screen and a control signal in accordance with the display command supplied thereto and supplies the signals to the switch 6. The switch 6 supplies an RGB signal from the OSD device 5 and a video signal from the video signal system block 3 and sends them at a predetermined timing to the CRT 4 in response to the control signal from the OSD device 5.

As a result, a new menu screen as shown in FIG. 5 is displayed on the CRT 4. On the menu screen, the item "ITEM 1" of the main menu and a sub menu of the "ITEM 1" of the main menu are displayed, and "ITEM 1-1" which is the first item of the sub menu is displayed highlighted. In

other words, the cursor is positioned at the "ITEM 1-1". Then, as described hereinabove, a manual operation of the cursor up key 20, the cursor down key 21, the decision key 22 or the menu key 23 is performed for the sub menu.

Thereafter, the control sequence advances to step S3 so that the processing at the steps beginning with step S3 is repeated.

On the other hand, if it is discriminated at step S12 that the predetermined item of the main menu whose selection has been settled by the decision key 22 does not have a sub menu positioned subordinate thereto, that is, if it is discriminated that the predetermined item is not an item at which movement of the cursor to next selection item should be performed but is an item at which predetermined processing which is an object for which predetermined control is to be performed, the control sequence advances to step S18.

At step S18, it is discriminated whether or not the item whose selection has been indicated is an item for setting the display of a sub menu to on or off. If it is discriminated that the item whose selection has been settled is an item for setting the display of a sub menu to on or off, the control sequence advances to step S19. At step S19, when the display of a sub menu is currently set in an on state, the display of a sub menu is set to off, but when the display of a sub menu is currently set in an off state, the display of the sub menu is set to on.

As a result, when a sub menu is displayed on the screen of the CRT 4, the sub menu is erased, but when no sub menu is displayed on the screen of the CRT 4, the sub menu is displayed newly. FIGS. 6A to 6C shows examples of a screen when the display of a sub menu is set to off. In particular, FIG. 6A shows an example of a screen when the cursor is positioned at the "ITEM 1" which is the first item of the main menu and the item is displayed highlighted. Similarly, FIG. 6B shows an example of a screen when the cursor is positioned at the "ITEM 2" and the item is displayed highlighted. FIG. 6C shows an example of a screen when the cursor is positioned at the "ITEM 3" and the item is displayed highlighted.

On the other hand, if it is discriminated at step S18 that the item whose selection has been indicated is not an item for setting the display of a sub menu to on or off, the control sequence advances to step S20, at which other processing is executed under the control of the CPU core 11. In particular, predetermined processing corresponding to the item whose selection has been indicated is executed. If it is recognized by the CPU core 11 that the processing is for setting a video mode of the television receiver as hereinafter described, then a corresponding instruction is supplied from the CPU core 11 to the bus data register 14. The instruction is supplied to the video signal system block 3 via the output port register 15 and the bus line 24. The video signal system block 3 generates and outputs a video signal corresponding to the indicate video mode in accordance with the instruction.

On the other hand, if it is discriminated at step S10 that the decision key 22 is not depressed, the control sequence advances to step S16, at which it is discriminated whether or not the menu key 23 is depressed. In the present embodiment, when the depressed key is not any one of the cursor up key 20, the cursor down key 21 or the decision key 22, it is the menu key 23, and consequently, it is discriminated that the menu key 23 is depressed and the control sequence advances to step S17. At step S17, the menu display is turned off.

To this end, the CPU core 11 produces a command for stopping the display of a menu screen and supplies the

command to the display command register 18. The command supplied to the display command register 18 is supplied to the OSD device 5 via the output port register 19 and the bus line 25. The OSD device 5 generates, in response to the command supplied thereto, a control signal for instructing the switch 6 to change over its internal connection of it so that, for example, a video signal from the video signal system block 3 may be supplied to the CRT 4, and supplies the control signal to the switch 6. As a result, only a video signal from the video signal system block 3 is supplied to the CRT 4, and no menu is displayed.

In this manner, by depressing the menu key 23, a menu of whichever hierarchy is currently displayed, the display of the menu can be ended. When it is desired to display the menu again, the menu key 23 should be depressed again. Accordingly, by depressing the menu key 23, the menu display can be alternately changed over between on and off.

Thereafter, the control sequence returns to step S1 so that the processing beginning with step S1 is repeated.

FIGS. 7 to 15 show different examples of a menu screen which can be used with the television receiver. The main menu is formed of items (icons) displayed on a left side portion of the screen, and here, the following items are displayed. In particular, they are items "VIDEO", "AUDIO", "PROG PALETTE", "INPUT OUTPUT", "TIMER", "SET UP" and "CC".

FIG. 7 shows a condition wherein the pointer (cursor) is positioned on the item "VIDEO" of the main menu and the item is displayed highlighted while a sub menu subordinate to the item is displayed. It can be understood from items of the displayed sub menu that various settings relating to an image can be performed by selective setting of the item "VIDEO" of the main menu.

Where, shown for example in FIG. 17 a remote commander 100 which will be hereinafter described is used, a select button 132 is first manually operated in an upward or downward direction to position the pointer to the item "VIDEO", and then the select button 132 is depressed in a vertical direction so that the selection of the item "VIDEO" can be indicated. This makes it possible to select a desired one of the items of the sub menu corresponding to the item "VIDEO" of the main menu. Consequently, by manually operating the select button 132 in an upward or downward direction, the pointer can be moved to a desired item of the sub menu, and then by depressing the select button 132 in a vertical direction, the item can be selected.

FIG. 8 illustrates a condition wherein the pointer is positioned on the item "AUDIO" of the main menu and the item is displayed highlighted while a sub menu positioned subordinate to the item is displayed. From the items of the displayed sub menu, it can be understood that various settings relating to sound can be performed by selective settlement of the item "AUDIO" of the main menu.

FIG. 9 illustrates a condition wherein the pointer is positioned on the item "PROG PALETTE" of the main menu and the item is displayed highlighted while a sub menu positioned subordinate to the item is displayed. From the items of the displayed sub menu, it can be understood that various settings relating to an image suitable to a kind of a program can be performed by selective settlement of the item "PROG PALETTE" of the main menu. Here, adjustment values of the "PICTURE" and the "COLOR CORRECTION" which can be set in FIG. 7 are set by the user in advance and are prepared as five different program palettes. Then, the user can select one of the palettes.

For example, if the item "MOVIE" of the sub menu is selected, then various adjustment values which can be set are

adjusted to values suitable for enjoyment of a program of a movie by settling the selection of the item "VIDEO" of the main menu as described hereinabove. Also with regard to each of the other items "STANDARD", "SPORTS", "NEWS" and "GAME", by selecting the item, the various adjustment values described above are adjusted to values suitable for enjoyment of an ordinary program, a sport program, a news program or a screen of a game.

FIG. 10 illustrates a condition wherein the pointer is positioned on the item "INPUT OUTPUT" of the main menu and the item is displayed highlighted while a sub menu positioned subordinate to the item is displayed. From the items of the displayed sub menu, it can be understood that various settings relating to an input and an output of the television receiver can be performed by selection of the item "INPUT OUTPUT" of the main menu. In the present embodiment, it is shown that a signal is output from a monitor output terminal (MONITOR OUT) of the television receiver and supplied to a video cassette recorder (VCR).

FIG. 11 illustrates a condition wherein the pointer is positioned on the item "TIMER" of the main menu and the item is displayed highlighted while a sub menu positioned subordinate to the item is displayed. From the items of the displayed sub menu, it can be understood that various settings relating to the time can be performed by selection of the item "TIMER" of the main menu.

FIG. 12 illustrates a condition wherein the pointer is positioned on the item "SETUP" of the main menu and the item is displayed highlighted while a sub menu positioned subordinate to the item is displayed. From the items of the displayed sub menu, it can be understood that various initial settings can be performed by selection of the item "SETUP" of the main menu.

FIG. 13 illustrates a condition wherein the pointer is positioned on the item "CC" of the main menu and the item is displayed highlighted while a sub menu positioned subordinate to the item is displayed. From the items of the displayed sub menu, it can be understood that various settings relating to a closed caption or a teletext can be performed by selection of the item "CC" of the main menu. For example, items "CC1" to "CC4" correspond to languages such as English and Spanish, and items "TEXT1" to "TEXT4" correspond to programs of a teletext.

Since the pointer moves on the main menu in response to a manual operation by a user and a sub menu which corresponds to a predetermined item on the main menu at which the pointer is positioned is displayed on a screen in this manner, it can be recognized immediately what setting can be performed by selection the item of the main menu. Accordingly, even if the user is unfamiliar with the operation of the television receiver, the relationship between the main menu and the sub menu can be understood simply, and desired setting can be performed rapidly.

FIG. 14 illustrates an example when the selection of the item "VIDEO" of the main menu is indicated and the pointer is moved to the item "PICTURE" of the sub menu corresponding to the item "VIDEO". Here, if the decision key 22 is depressed to indicate the selection of the item "PICTURE", then the adjustment values of the item "PICTURE" can be set.

FIG. 15 illustrates an example when the selection of the item "CC" is indicated and the pointer is moved to the item "CC1" of the sub menu corresponding to the item "CC". Here, if the decision key 22 is depressed to indicate the selection of the item "CC1", then the television receiver is set so that a closed caption in a predetermined language corresponding to the item "CC1" may be displayed.

FIG. 16 is a block diagram showing a construction of another television receiver to which a second embodiment of the present invention is applied. The television receiver of the present embodiment is a modification to and includes common components to those of the television receiver of the first embodiment described hereinabove with reference to FIG. 1, and accordingly, overlapping description of the common construction is omitted here to avoid redundancy. The television receiver of the present embodiment is different from the television receiver of the preceding embodiment only in that the body key apparatus 2 additionally includes a sub menu key 26 which can input an instruction to change over the display of a sub menu between on and off. If the sub menu key 26 is depressed, then corresponding key data is supplied to and stored into the key detection register 13. The key data is read out by the CPU core 11, and in response to the key data, if the display of a sub menu is currently set on, then the display of the sub menu is set to off, but if the display of a sub menu is currently set off, the display of the sub menu is set to on. Then, when it becomes necessary to re-write the screen as a result of the re-setting of the display of a sub menu, contents of the display command register 18 are re-written by the CPU core 11.

FIG. 17 shows an example of a construction of a button switch arrangement of a remote commander which can be used to operate such a television receiver as shown in FIG. 1. A muting button switch 102 is manually operated to set or cancel a muting condition of the CRT 4. A sleep button switch 103 is manually operated to set or cancel a sleep mode in which the power supply is automatically interrupted when a predetermined point of time comes or when a predetermined time elapses.

When a cable power source button switch 104, a DSS (Digital Satellite System) power source button switch 105 and a television power source button switch 106 are manually operated, a cable box (not shown), a receiver (not shown) for receiving a DSS and the power source for the television receiver are switched off, respectively.

A cable button switch 110, a DSS button switch 111 and a television button switch 112 are button switches for changing over between functions, that is, for changing over between apparatus categories by transmitting a code of an infrared ray signal emitted from a light emitting element 101 of the remote commander 100. In particular, the cable button switch 110 is manually operated when a signal transmitted via a cable and received by the cable box is to be displayed on the CRT 4. In response to the manual operation of the cable button switch 110, a code of an apparatus category allocated to the cable box is emitted as an infrared ray signal. Similarly, the DSS button switch 111 is manually operated when a digital satellite broadcast received via an artificial satellite is to be displayed on the CRT 4. The television button switch 112 is manually operated when a signal received by the tuner (not shown) is to be displayed. LEDs 107, 108 and 109 are lit when the cable button switch 110, the DSS button switch 111 and the television button switch 112 are turned on, respectively. Consequently, it is indicated that, when a button is depressed, to an apparatus of which category a code is transmitted.

A PIP (picture-in-picture) display button switch 114, 115 or 116 is manually operated when a picture-in-picture screen is to be displayed at a predetermined position of the screen of the CRT 4. An OFF button switch 113 is manually operated when the display of a picture-in-picture displayed on the screen is to be ended. An AUDIO button switch 117 is manually operated when an audio output is to be changed over between sound corresponding to an image displayed on the picture-in-picture screen and sound corresponding to an image displayed on the ordinary screen.

A SWAP button switch 118 is manually operated when an ordinary screen and a picture-in-picture screen are to be swapped. A position button switch 119 is manually operated when the position of the screen at which a picture-in-picture screen is to be displayed is to be designated such as, for example, a right upper position, a right lower position, a left upper position or a left lower position of the screen. A television/video change-over button switch 120 is manually operated when a signal to be displayed on the picture-in-picture screen is to be changed over to a signal from the tuner built in the television receiver or an input signal (from a VCR or the like) from a video input terminal. A channel up/down button switch 121 is manually operated when a channel to be displayed on the picture-in-picture screen is to be changed over. A FREEZE button switch 122 is manually operated when an image displayed on the picture-in-picture screen is to be changed to a still picture.

Another television/video change-over button switch 123 is manually operated when a signal to be displayed on the ordinary screen is to be changed over to the signal from the tuner built in the television receiver or to an input signal (from a VCR or the like) from the video input terminal. An antenna/AUX change-over button switch 124 is manually operated to change over an input between an antenna input and an AUX input.

A jump button switch 125 is manually operated to restore an original channel which was received prior to the changing over between the antenna input and the AUX input. Each of numeric button (ten key) switches 126 on which numerals from 0 to 9 are indicated is manually operated when a number indicated thereon is to be inputted. An enter button switch 128 is manually operated after manual operation of the numeric button switches 126 is completed in order to input ending of inputting of a number. When a channel is changed over, a banner including a number, a call sign (name), a logo and a main icon of the new channel is displayed, for example, for 3 seconds. Here, two banners are available including a banner of a simple construction which includes the elements mentioned above and another banner of a more detailed construction which includes, in addition to the elements mentioned above, a name and a broadcast starting time of a program, the present time and so forth. A display button switch 127 is manually operated when the type of a banner to be displayed is to be changed over.

A volume button switch 129 is manually operated when the volume of sound is to be increased or decreased. A menu button switch 130 (menu display instruction means) is manually operated when a menu screen is to be displayed on the CRT 4 or when such display of a menu screen is to be ended. A channel up/down button switch 131 is manually operated when the number of a broadcasting channel to be received is to be increased or decreased.

The select button 132 (designation means, lower menu display instruction means, first selection means, second selection means) not only can be manually operated (directional operation) totaling eight directions including upward, downward, leftward and rightward directions and four intermediate oblique directions, but also can be manually operated or depressed (operation for selection) in a vertical direction with respect to the top face of the remote commander 100.

FIG. 18 shows an example of a construction of a small stick switch which is used as the select button 132. The small stick is so structured that a lever 202 extends from a body 201. When the select button 132 is directionally operated in one of the eight directions in a horizontal plane, it is pivoted in the operation direction. Further, when the select button 132 is manually operated for selection (operated vertically), the lever 202 is pushed down in a vertical direction.

FIG. 19 shows the eight operation directions of the lever 202 in a horizontal plane. As seen from FIG. 19, the lever

202 can be directionally operated in the eight directions indicated by A to H in the horizontal plane.

FIG. 20 shows an example of an internal construction of the remote commander 100. Referring to FIG. 19, contacts A to H in the inside of the body 201 of the small stick switch correspond to the eight directions A to H shown in FIG. 19. When the lever 202 is manually operated in one of the directions A to D, a corresponding one of the contacts A to D is connected to a terminal C1. On the other hand, when the lever 202 is pivoted in one of the directions E to H, a corresponding one of the terminals B to H is connected to another terminal C2. Further, between the terminals H and A and between the terminals D and E, both of the terminals C1 and C2 are connected to them, respectively. Further, when the lever 202 is manually operated in a vertical direction, the terminals C1 and C2 are connected to each other.

The connection condition of the terminals of the body 201 is monitored by a CPU 204 of a microcomputer 203. Consequently, the CPU 204 can detect a directional operation and a selection operation of the select button 132.

Further, the CPU 204 always scans a button switch matrix 209 to detect a manual operation of any other button switch of the remote commander 100 shown in FIG. 17.

The CPU 204 executes various processing in accordance with a program stored in a ROM 205 and suitably stores necessary data into a RAM (Random Access Memory) 206.

When an infrared ray signal is to be outputted, the CPU 204 drives a LED 208 via a LED driver 207 so that an infrared ray signal may be outputted from the LED 208.

For example, if a menu button 130 is depressed, then a corresponding infrared ray signal is emitted from the light emitting element 101 and received by a light receiving element (not shown) of the television receiver shown in FIG. 1. The signal is supplied to the CPU core 11, by which a display command for displaying a predetermined menu screen is placed into the display command register 18. The display command placed in the display command register 18 is supplied to the OSD device 5 via the output port register 19 and the bus line 25. The OSD device 5 generates an RGB signal corresponding to the menu screen and a control signal in response to the display command supplied thereto and supplies the signals to the switch 6. The switch 6 supplies the RGB signal from the OSD device 5 or a video signal from the video signal system block 3 to the CRT 4 changing over them at a predetermined timing in response to the control signal from the OSD device 5. As a result, a menu screen is displayed on the screen of the CRT 4 in a superposed condition with a program of an ordinary television broadcast as shown in FIG. 3.

At first, the cursor is positioned at the "ITEM 1" which is the first item of the main menu and the "ITEM 1" is displayed highlighted while a sub menu corresponding to the "ITEM 1" is simultaneously displayed. If the select button 132 is manually operated, in this condition, in a downward direction in FIG. 19, then the cursor moves to the position of the "ITEM 2" as seen in FIG. 4A and the "ITEM 2" is highlighted displayed. Further, a sub menu corresponding to the "ITEM 2" is simultaneously displayed. Then, if the select button 132 is manually operated in the downward direction again, then the cursor moves to the position of the "ITEM 3" and the "ITEM 3" is displayed highlighted while a sub menu corresponding to the "ITEM 3" is simultaneously displayed. In this manner, by manually operating the select button 132, a sub menu corresponding to any item of the main menu can be displayed.

If, for example, the select button 132 is manually operated to position the cursor at the "ITEM 1" and then manually operated in the vertical direction, then the selection of the

"ITEM 1" is selected. As a result, the cursor moves to the first item "ITEM 1-1" among items forming a sub menu corresponding to the "ITEM 1" and the "ITEM 1-1" is displayed highlighted. Here, by manually operating the select button 132 in an upward or downward direction, the cursor can be positioned at a desired one of the items of the sub menu. Then, by manually operating the select button 132 in the vertical direction, the selection of the highlighted displayed item can be selected.

Further, when the display of a sub menu is to be set to on (to be displayed) or off (not to be displayed), for example, the item "ITEM 4" of the main menu in FIG. 3 is determined as an item for changing over between on/off of a sub menu display, and the select button 132 is manually operated to move the cursor to the item "ITEM 4" and then manually operated in the vertical direction to indicate the selection of the "ITEM 4". Consequently, the display of the sub menu is turned off.

As a result, even if the cursor is positioned at one of the items of the main menu and the item is displayed highlighted, a sub menu corresponding to the item is not displayed. In order to set the display of a sub menu to on, operation similar to that described hereinabove is performed so that the display of the sub menu can be set to on.

By setting the display of a sub menu to off, possible obstruction of it to enjoyment of a program of a television broadcast displayed on the screen can be minimized. Further, to a user who understands the menu structure well, elimination of an unnecessary display can improve the convenience for use.

FIG. 21 shows in schematic view another remote commander for a television receiver to which the present invention is applied. The present remote commander is a modification to and is basically common with the remote commander described hereinabove with reference to FIG. 17 in terms of the arrangement of buttons, the internal construction and the operation, and overlapping description thereof is omitted here to avoid redundancy. The present remote commander is different from the remote commander of FIG. 17 only in that it additionally includes a sub menu button 133 (lower menu display instruction means) for exclusive use for turning the display of a sub menu on or off. A user can set the display of a sub menu to on or off by depressing the sub menu button 133.

It is to be noted that, while the menu system in any of the television receivers of the embodiments described hereinabove includes two hierarchies of the main menu and sub menus, it may otherwise include an arbitrary number of hierarchies equal to or greater than 3. In this instance, menus of all hierarchies may be displayed on a screen or menus of only a predetermined number of ones of the hierarchies may be displayed on a screen.

Further, while the main menu in any of the television receivers of the embodiments described hereinabove is displayed on the left side portion of the screen while a sub menu is displayed on the right side portion of the screen, they may otherwise be displayed at other arbitrary positions.

Further, while, in any of the television receivers of the embodiments described above, items forming the main menu or a sub menu are arranged in a vertical column, they may otherwise be arranged in a horizontal row.

Further, while a sub menu on any of the television screens of the embodiments described above is displayed in the form of characters, it may otherwise be displayed in the form of button icons or the like.

Further, while the pointer displayed on any screen shown in the drawings is shown having the shape of a finger, it may have the shape of an arrow mark or may have any other arbitrary shape.

Having now fully described the invention, it will be apparent to one of ordinary skill in the art that many changes and modifications can be made thereto without departing from the spirit and scope of the invention as set forth herein.

What is claimed is:

1. A function selection method for a television receiver comprising the steps of:
displaying a first level of a hierarchical menu in a first region of a screen of said television receiver, wherein a plurality of selection items corresponding to functions of said television receiver are displayed;
designating one of said plurality of selection items from said first level of said hierarchical menu displayed on said screen of said television receiver;
displaying a subordinate level of said hierarchical menu in a second region of said screen, wherein a plurality of control items corresponding to said designated selection item are displayed;
selecting said designated selection item of said first level of said hierarchical menu;
selecting one of said plurality of control items from said subordinate level of said hierarchical menu; and
modifying said selected control item, whereby said functions of said television receiver corresponding to said designated selection item is controlled by modifying said selected control item.
2. The function selection method according to claim 1 wherein a number of levels of hierarchy of said hierarchical menu is equal to or greater than 2.
3. A function selection method for a television receiver comprising the steps of:
displaying a first level of a hierarchical menu indicating a plurality of selection items corresponding to functions of said television receiver in a first region of a screen of said television receiver;
designating one of said plurality of selection items from said first level of said hierarchical menu displayed on said screen of said television receiver;
selecting said designated selection item;
displaying a subordinate menu in a second region of said screen of said television receiver indicating further selection items corresponding to a further set of functions of said television receiver related to the designated selection item; and
selecting one of the selection items from said subordinate menu, whereby said further set of selection items is used to control said further set of functions of said television receiver.
4. The function selection method according to claim 3, wherein said number of the hierarchies of said hierarchical menu is equal to or greater than 2.
5. A television receiver, comprising:
menu display means for displaying selection items of a first level of a hierarchical menu which includes a plurality of selection items corresponding to functions of said television receiver in a first region of a screen of said television receiver;
designation means for designating one of said selection items of said first hierarchical level of the menu displayed by said menu display means;
subordinate menu display means for displaying a subordinate hierarchical level of said menu which includes a

plurality of control items for controlling a function corresponding to said designated selection item of said first hierarchical level in a second region of said screen of said television receiver;

- first selection means for selecting said selection item designated by said designation means;
- second selection means for selecting one of said plurality of control items from said subordinate menu related to said selection item selected by said first selection means; and
modifying means for modifying said control item, whereby said functions of said television receiver corresponding to said selected selection item is modified.
6. The television receiver according to claim 5 wherein a number of hierarchical levels of said menu is equal to or greater than 2.
7. The television receiver according to claim 5 further comprising a setting means responsive to said menu display means for preventing said subordinate menu display means from displaying said subordinate hierarchical level of said menu.
8. A remote commander for a television receiver comprising:
menu display instruction means for causing said television receiver to display a first level of a hierarchical menu in a first region of a screen of said television receiver, wherein selection items of said first level of said hierarchical menu correspond to functions of said television receiver and, wherein at least one subordinate hierarchical level of said menu corresponds to control of said functions of said television receiver;
designation means for causing said television receiver to designate one of said selection items of said first hierarchical level of said menu displayed by said television receiver in response to said menu display instruction means;
- subordinate menu display instruction means for causing said television receiver to display said subordinate hierarchical level in a second region of said screen of said television receiver while said selection items of said first hierarchical level of said menu are displayed in said first region of said screen in response to the instruction of said menu display instruction means, wherein said control functions of said subordinate level of said menu correspond to designated selection items of said first level of said menu;
- first selection means for selecting said selection item designated by said designation means; and
second selection means for selecting one of said control functions of said subordinate menu.
9. The remote commander for a television receiver according to claim 8 wherein a number of the hierarchies of said menu is equal to or greater than 2.
10. The function selection method according to claim 1 wherein said first and second screen regions do not overlap.
11. The function selection method according to claim 3 wherein said first and second screen regions do not overlap.
12. The television receiver according to claim 5 wherein said first and second screen regions do not overlap.
13. The remote commander according to claim 8 wherein said first and second screen regions do not overlap.

* * * * *

EXHIBIT F



US006661472B2

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Shintani et al.

(10) Patent No.: **US 6,661,472 B2**
(45) Date of Patent: *Dec. 9, 2003

(54) CHANNEL SELECTION IN DIGITAL TELEVISION

(75) Inventors: Peter Rae Shintani, San Diego, CA (US); Shigeharu Kondo, San Diego, CA (US)

(73) Assignees: Sony Corporation, Tokyo (JP); Sony Electronics Inc., Park Ridge, NJ (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/406,541

(22) Filed: Sep. 27, 1999

(65) Prior Publication Data

US 2003/0133050 A1 Jul. 17, 2003

Related U.S. Application Data

(60) Provisional application No. 60/102,942, filed on Sep. 30, 1998.

(51) Int. Cl.⁷ H04N 5/445; H04N 5/54; H04N 7/00; H04N 5/50

(52) U.S. Cl. 348/732; 348/731; 348/569; 348/563; 725/57; 725/56

(58) Field of Search 348/731, 734, 348/385.1, 386.1, 569, 906, 563, 553, 572, 570; 725/56, 44, 151, 20, 57

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Primary Examiner—Michael H. Lee

Assistant Examiner—Paulos M. Natnael

(74) Attorney, Agent, or Firm—John L. Rogitz

(57) ABSTRACT

Methods and apparatus implementing a technique for selecting a channel in a digital television. In one implementation, selecting a channel includes: receiving a major and minor channel number sequence, including a major channel number, a delimiter, and a minor channel number, where the delimiter separates the major channel number and the minor channel number; identifying a physical channel which corresponds to the major and minor channel number sequence by accessing a channel look up table, where the channel look up table includes correspondences between major and minor channel number sequences and physical channels; identifying a virtual channel table which corresponds to the physical channel, where the virtual channel table indicates a virtual channel which corresponds to the major and minor channel number sequence; tuning to the physical channel to receive a signal carried on the physical channel; and decoding the virtual channel from the tuned signal.

18 Claims, 7 Drawing Sheets

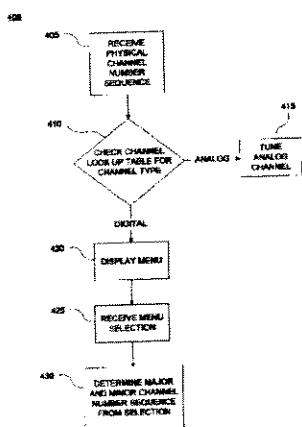


FIG. 1A

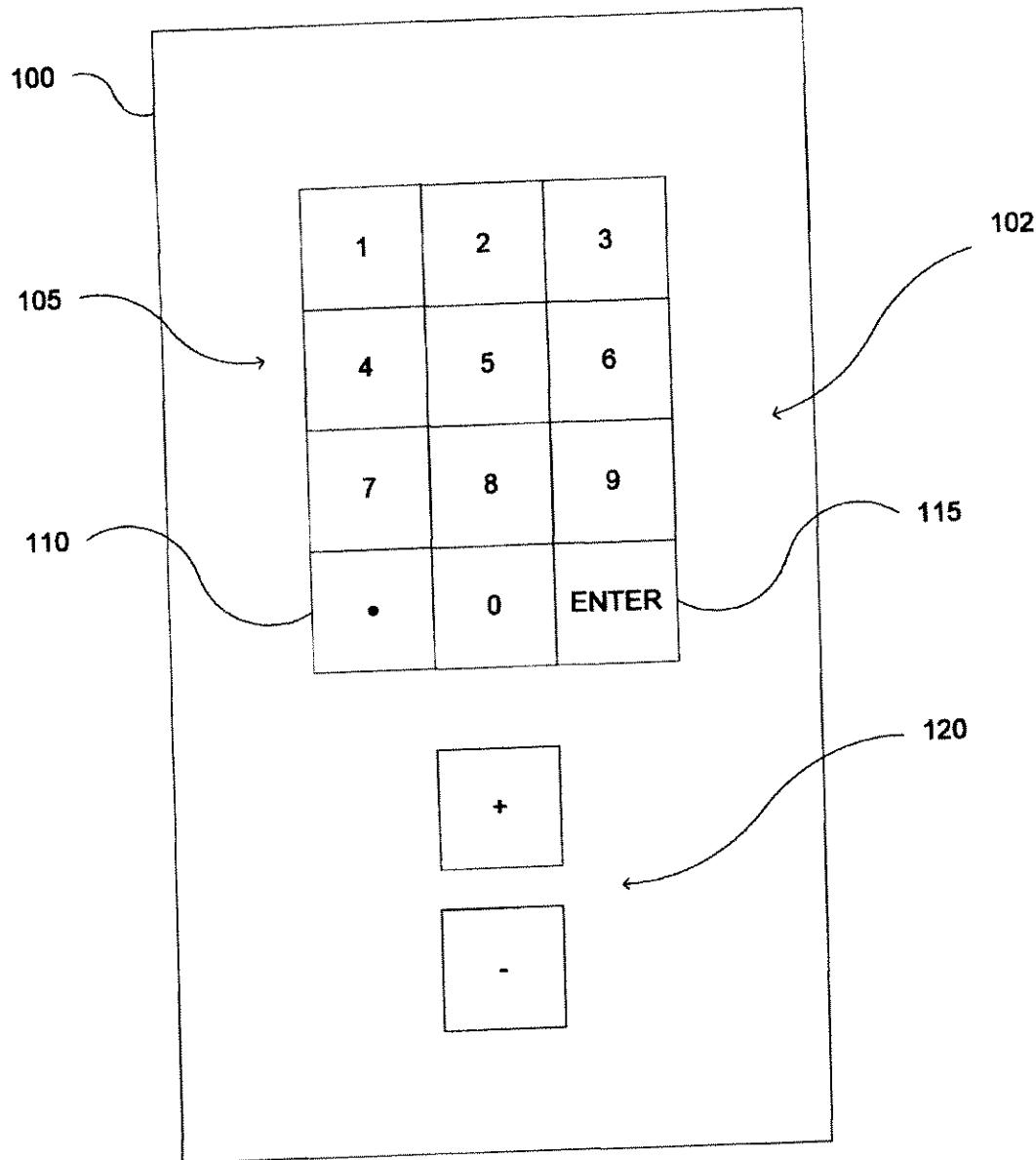


FIG. 1B

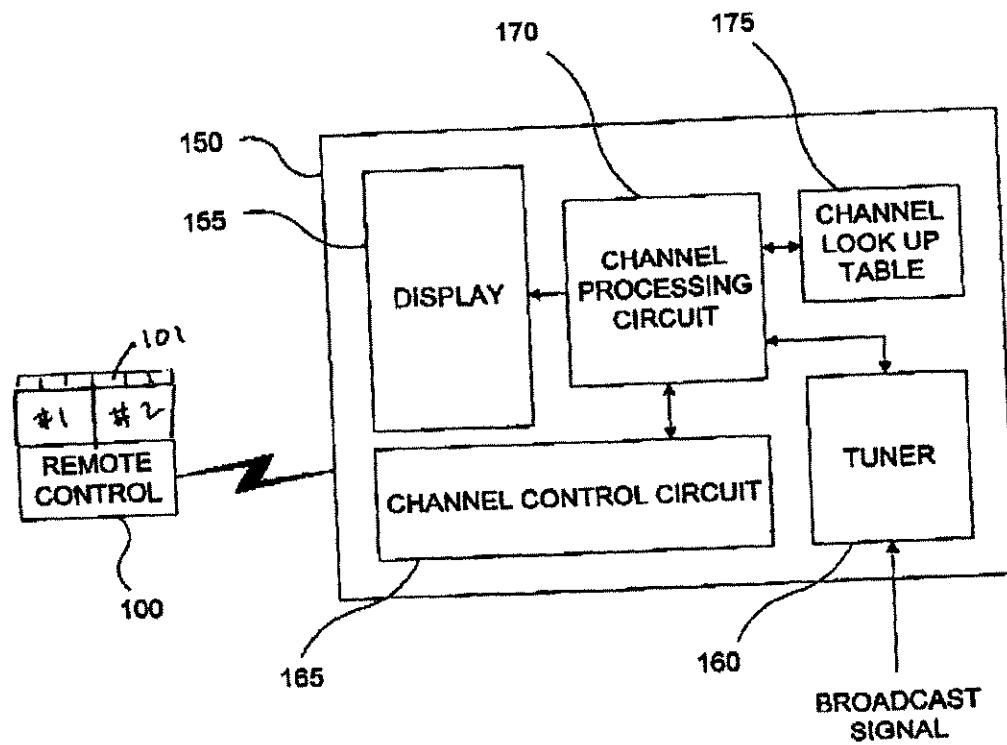


FIG. 2A

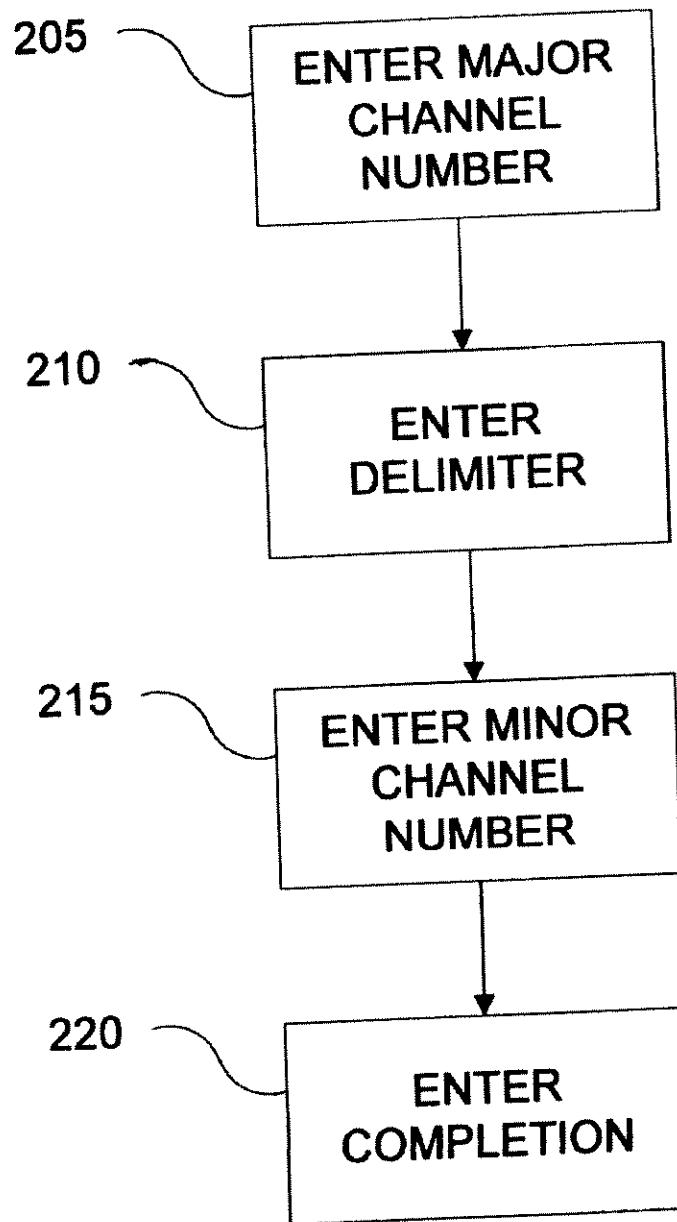
200

FIG. 2B

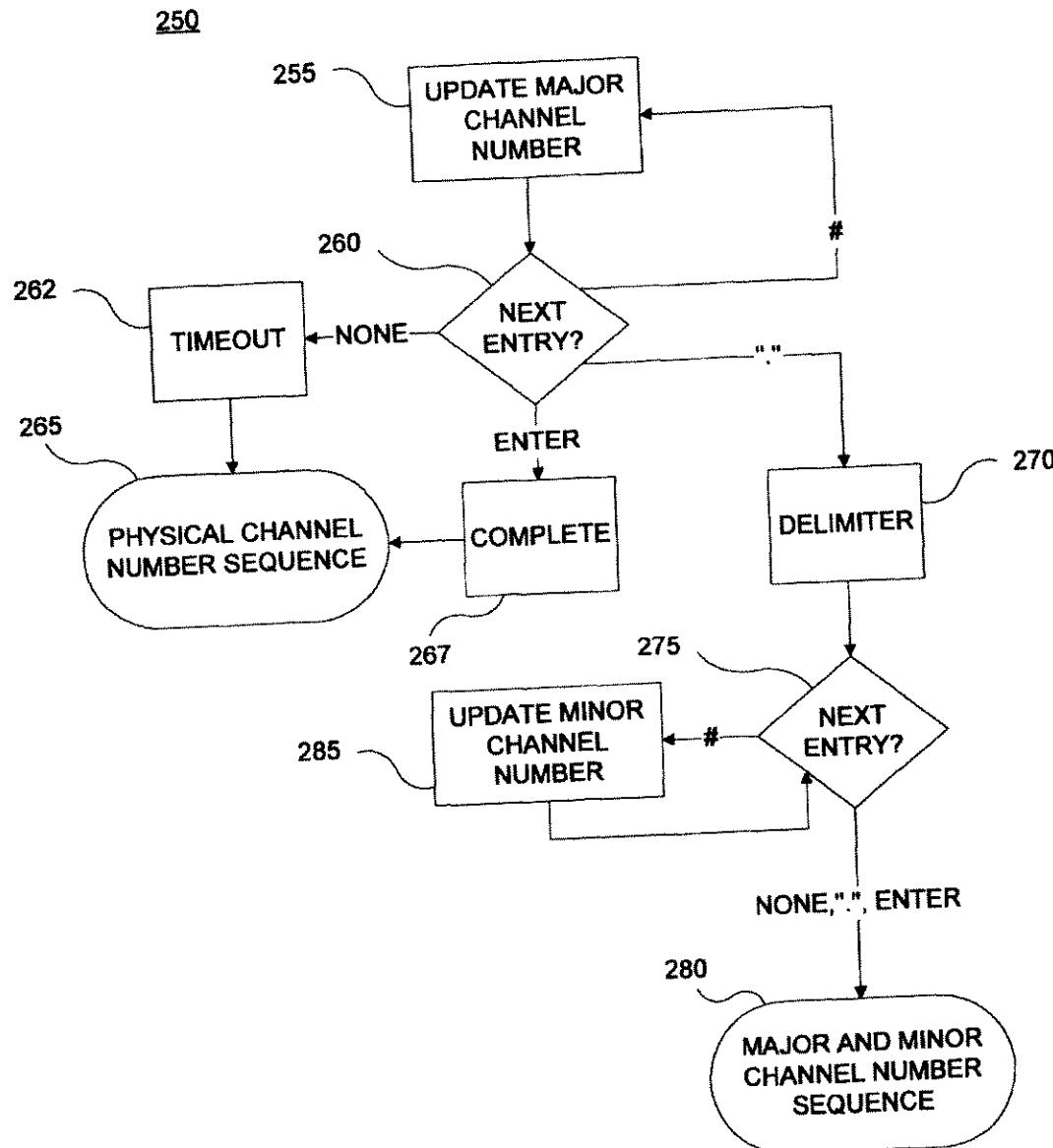


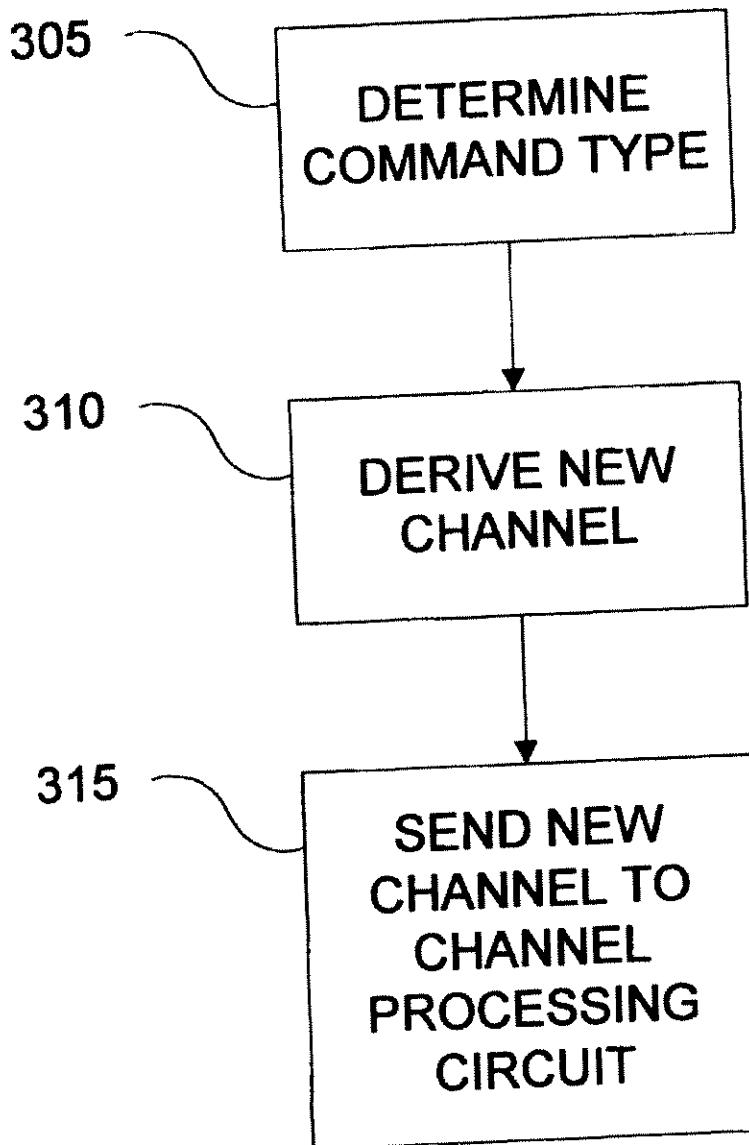
FIG. 3300

FIG. 4

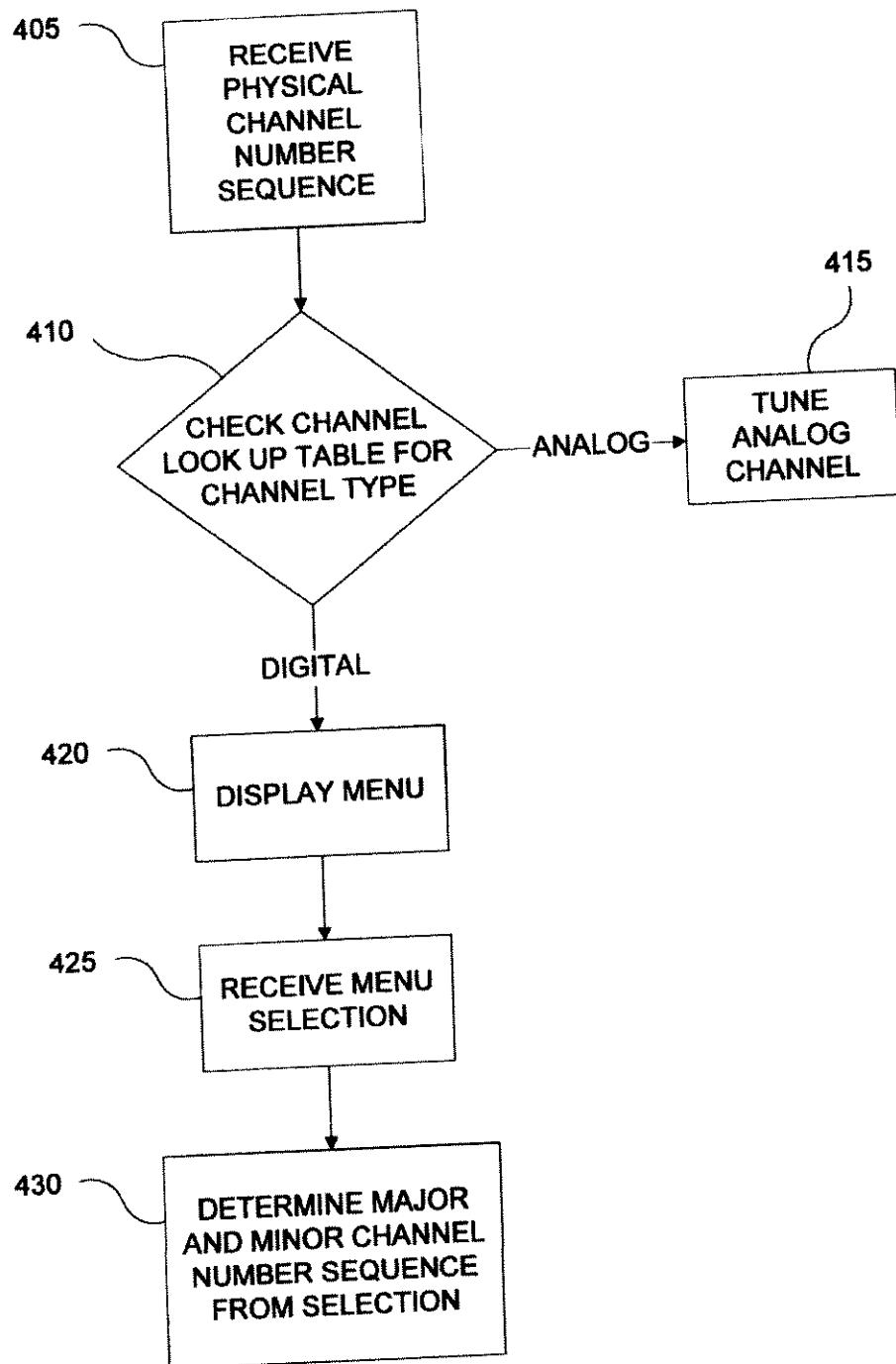
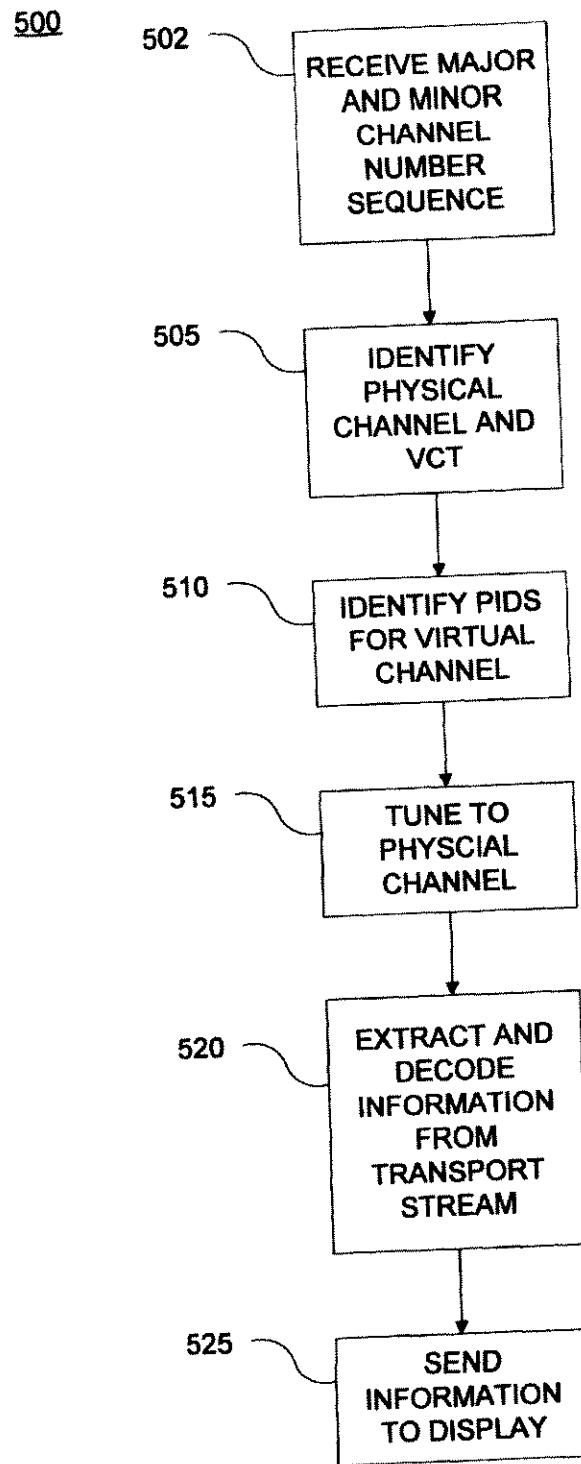
400

FIG. 5



1 CHANNEL SELECTION IN DIGITAL TELEVISION

This application claims the benefit of U.S. Provisional Application No. 60/102,942, filed Sep. 30, 1998.

BACKGROUND

To view a television program being transmitted to a user's television, the user provides a channel number to the television. In conventional analog broadcast television, this channel number is a reference to a particular frequency band at which the analog signal carrying the television program is broadcast. This frequency band is also referred to as a "physical channel." The channel number identifies from which frequency band a tuner in the television is to receive. Thus, a channel number indicates a physical channel and the associated program.

In digital broadcast television, a frequency band can carry a signal which is an encoded digital transport stream. When decoded, the transport stream can include one or more streams having various forms of content, such as video or audio for a program, text based information, closed captioning, or any information which can be transmitted digitally. Each of these items can be associated with a different channel number. Accordingly, a single physical channel can include multiple items or "virtual channels." In this case, a channel number refers to a virtual channel, a particular item encoded within a transport stream, instead of referring to a physical channel.

In addition, content in a transport stream can be related to content broadcast as an analog signal or in a different transport stream. For example, a transport stream can include a high definition television ("HDTV") version of a program that is also broadcast as an analog signal at a different unrelated frequency band.

SUMMARY

The invention provides methods and apparatus implementing a technique for selecting a channel in a digital television. In one implementation, selecting a channel includes: receiving a major and minor channel number sequence, including a major channel number, a delimiter, and a minor channel number, where the delimiter separates the major channel number and the minor channel number; identifying a physical channel which corresponds to the major and minor channel number sequence by accessing a channel look up table, where the channel look up table includes correspondences between major and minor channel number sequences and physical channels; and identifying a virtual channel table which corresponds to the physical channel, where the virtual channel table indicates a virtual channel which corresponds to the major and minor channel number sequence. Selecting a channel can further include: tuning to the physical channel to receive a signal carried on the physical channel; and decoding the virtual channel from the tuned signal.

In another aspect, an input device for selecting a channel in a digital television includes: a keypad including a plurality of number keys for inputting respective numbers; and a delimiter key for inputting a delimiter, where a channel is indicated by a major and minor channel number sequence which includes a major channel number input through one or more number keys of the keypad, a delimiter input through the delimiter key, and a minor channel number input through one or more number keys of the keypad.

In another aspect, a digital television includes: a display; a tuner including a connection for an externally supplied

broadcast signal, where the tuner provides a signal carried on a physical channel selected from the broadcast signal; a channel control circuit which derives major and minor channel number sequences from received control signals, 5 where a major and minor channel number sequence indicates a specific channel carried in the broadcast signal; a channel processing circuit connected to the channel control circuit, the display, and the tuner, where the channel processing circuit causes the tuner to select a physical channel corresponding to the major and minor channel number sequence supplied by the channel control circuit and provide 10 a digital signal carried thereon, decodes a channel indicated by the major and minor channel number sequence in the digital signal, and supplies the decoded channel to the display.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A shows a hand-held remote control which provides efficient input of major and minor channel numbers to 20 select a channel on a digital television.

FIG. 1B shows a remote control and a digital television.

FIG. 2A is a flowchart of a process for directly entering channel numbers for a major and minor channel number sequence using a keypad.

FIG. 2B is a flowchart of a process for processing number sequences entered using a keypad.

FIG. 3 shows a process for selecting a channel using channel commands.

FIG. 4 is a flowchart of a process for selecting a virtual channel through a menu shown on a display.

FIG. 5 is a flowchart of a process for processing major and minor channel number sequences in a digital television.

DETAILED DESCRIPTION

35 The Advanced Television System Committee ("ATSC") established a standard protocol for transmission of data tables for use with digital television. This protocol is referred to as the Program and System Information Protocol ("PSIP") and is described in "Program and System Information Protocol for Terrestrial Broadcast and Cable," document A/65, Dec. 23, 1997 published by the ATSC. The information describing the content of a transport stream for a physical channel is referred to as the PSIP for that physical channel.

40 In digital television, each channel in a transport stream is a virtual channel associated with a major channel number and a minor channel number. A major channel number can be used to identify channels which belong to a common broadcast corporation or other group. A minor channel number specifies a particular channel in such a group. In one example, all the virtual channels in a transport stream have the same major channel number and have respective minor channel numbers. In addition, virtual channels can have as 45 a major channel number the channel number of a physical channel carrying a related analog channel (analog channels do not need minor channel numbers). In another example, a program is transmitted as an analog signal on physical channel 2. The HDTV version of the same program is transmitted in a transport stream, such as within an unrelated frequency band on a different physical channel, and the virtual channel for that HDTV program has the major channel number 2. Thus, a physical channel can be indicated by a major channel number and a virtual channel can be indicated by a major and minor channel number pair.

50 55 60 65 65 The PSIP describes the information for all the virtual channels in a transport stream. The PSIP includes a virtual

channel table ("VCT") which describes the correspondence between major and minor channel numbers and the virtual channels. A digital television uses the VCT to interpret a user's input to select the appropriate major and minor channel number and hence the desired virtual channel.

FIG. 1A shows an implementation of an input device as a hand-held remote control 100 which provides efficient input of major and minor channel numbers to select a channel on a digital television. Remote control 100 includes at least one keypad 102. Keypad 102 includes one or more number keys 105, such as 10 number keys labeled 0-9, a delimiter key 110, an enter key 115, and one or more channel command keys 120, such as keys labeled with plus ("+") and minus ("-"). In an alternative implementation, a keypad includes alphanumeric keys so that a user can enter combinations of letters and/or numbers to identify a channel, such as "SNN.HDTV". Alphanumeric labels can be set by the user or provided automatically, such as through a broadcast signal in a transport stream.

A user enters channel numbers by depressing one or more number keys 105. A user indicates the separation between a major channel number and a minor channel number by depressing delimiter key 110. A sequence of a major channel number, a delimiter, and a minor channel number is a major and minor channel number sequence. Because delimiter key 110 is provided on remote control 100, a user can conveniently enter a major and minor channel number sequence to access a specific channel directly.

Delimiter key 110 is marked with a delimiter. In FIG. 1A, delimiter key 110 is marked with a dot ("."). This delimiter can take any form, for example, and not by way of limitation, a slash (""/), a space (" "), or a dash ("--"). The choice of a dot as the delimiter is advantageous as being a familiar break in numeric representation in the decimal system. In one implementation, the delimiter is implemented as a predetermined break or arrangement of memory storage, rather than a separately stored character. In another implementation, the delimiter is indicated by inputting a major channel number with a first keypad and a minor channel number with a second keypad (shown in FIG. 1B).

To complete a channel number entry, the user can depress enter key 115. An automatic timeout can also complete a channel number entry if the user does not depress any key for a specified period. The user enters channel commands by depressing one of one or more channel command keys 120, such as to change to a sequentially adjacent channel. For example, in one implementation, to change from the current channel to the sequentially next channel, the user can depress a channel command key 120 marked with a plus ("+").

FIG. 1B shows remote control 100 and a digital television 150, with the control 100 potentially having one or more keypads (two shown) and alphabet keys 101. Digital television 150 includes a display 155, such as a cathode ray tube ("CRT"), a tuner 160, a channel control circuit 165, and a channel processing circuit 170. These components can be implemented separately or in combination. In one implementation, digital television 100 also includes an integrated keypad for entry of channel numbers and commands directly into digital television 150.

Remote control 100 sends control signals to digital television 150 according to keys depressed by the user. Channel control circuit 165 receives the control signals. Channel control circuit 165 recognizes channel commands or combinations of channel numbers and delimiters to select a desired physical or virtual channel. For example, in an

implementation where the delimiter is a dot, channel control circuit 165 recognizes the sequence "4.2" as a request for major channel number 4 and minor channel number 2. Channel selection is described further below with respect to FIGS. 2A through 5. Channel control circuit 165 provides channel information, such as major and minor channel numbers, to channel processing circuit 170.

Channel processing circuit 170 uses the channel information from channel control circuit 165 and information stored in a channel look up table 175 to determine the desired physical or virtual channel. Channel look up table 175 is implemented as writeable memory, such as RAM or flash ROM. Channel processing circuit 170 creates channel look up table 175 during initialization of digital television 150 and updates channel look up table 175 dynamically. Channel look up table 175 defines correspondences between major and minor channel numbers and physical and virtual channels. The allocation of minor channel numbers is derived from information obtained from the PSIP of digital physical channels. Major channel numbers correspond to physical channels, which may be different from the physical channels carrying the transport streams. Channel look up table 175 also indicates whether each physical channel is an analog channel or a digital channel.

Channel processing circuit 170 causes tuner 160 to select a physical channel from a broadcast signal received at digital television 150. The broadcast signal can be received through various reception systems, such as an antenna, a cable system (e.g., CATV), or a satellite system (e.g., DSS). Tuner 160 provides a signal on the selected physical channel to channel processing circuit 170.

When the channel information indicates a physical channel is desired, such as an analog channel, channel processing circuit 170 passes the signal from tuner 160 to display 155 unchanged. When the channel information indicates a virtual channel is desired, channel processing circuit 170 performs appropriate digital signal processing to extract information from a transport stream based on information supplied in the VCT. For example, channel processing circuit 170 can extract and decode, using decoding such as MPEG-2, a video signal and an audio signal from a transport stream which corresponds to a desired virtual channel. Channel processing circuit 170 provides the signal or signals to display 155.

FIG. 2A is a flowchart of a process 200 for directly entering channel numbers for a major and minor channel number sequence using a keypad, such as keypad 102 shown in FIG. 1A. A user enters a major channel number by depressing an appropriate number key or keys 105 (205). The user enters a delimiter by depressing delimiter key 110 (210). As discussed above, the delimiter indicates the end of the major channel number. For example, the delimiter allows a user to enter directly and distinguishably the sequences "42.3" and "4.23." The user enters a minor channel number by depressing an appropriate number key or keys 105 on remote control 100 (215). The user completes the sequence by depressing enter key 115 (220). The major channel number, delimiter, and minor channel number can be supplied to the channel control circuit separately or together.

FIG. 2B is a flowchart of a process 250 for processing number sequences entered using a keypad, such as keypad 102 shown in FIG. 1A, to generate a channel number sequence in a digital television, such as in channel control circuit 165 shown in FIG. 1B. As described above, a major and minor channel number sequence includes a major channel number, a delimiter, and a minor channel number. A physical channel number sequence includes a channel number.

When channel control circuit 165 receives an entry of a channel number, and is not already processing another channel number sequence, channel control circuit stores the received number as the first digit of a current channel number (255). Channel control circuit 165 causes display 155 to display the received channel number and entries as entries are received for user feedback. Channel control circuit 165 waits to receive another entry for a specified timeout period (260). If channel control circuit 165 does not receive another entry before the timeout period expires (262), channel control circuit 165 passes the current channel number to channel processing circuit 170 as a physical channel number sequence (265). If channel control circuit 165 receives a completion signal, such as from enter key 115, before the timeout period expires (267), channel control circuit 165 passes the current channel number to channel processing circuit 170 as a physical channel number sequence (265).

If channel control circuit 165 receives another channel number before the timeout period expires, channel control circuit 165 concatenates the new channel number with the current channel number as the next digit (255). Channel control circuit 165 resets the timeout period to wait for another entry (260).

If channel control circuit 165 receives a delimiter before the timeout period expires, channel control circuit 165 concatenates the delimiter with the current channel number (270). Channel control circuit 165 resets the timeout period to wait for another entry (275).

If channel control circuit 165 does not receive another entry before the timeout period expires, channel control circuit 165 passes the current channel number to channel processing circuit 170 as a major and minor channel number sequence (280). If the current channel number ends with a delimiter, channel control circuit 165 concatenates a default value, such as zero, with the current channel number before passing the current channel number to channel processing circuit 170.

Similarly, if channel control circuit 165 receives a completion signal, such as from enter key 115, or a second delimiter before the timeout period expires, channel control circuit 165 passes the current channel number to channel processing circuit 170 as a major and minor channel number sequence (280). If the current channel number ends with a delimiter, channel control circuit 165 concatenates a default value, such as zero, with the current channel number before passing the current channel number to channel processing circuit 170.

If channel control circuit 165 receives another channel number before the timeout period expires, channel control circuit 165 concatenates the new channel number with the current channel number as the next digit (285). Channel control circuit 165 resets the timeout period to wait for another entry (275).

For example, to select physical channel 2, an analog channel, a user enters "2" with a number key 105 and then "ENTER" with enter key 115 using remote control 100 as shown in FIG. 1A. To select virtual channel 4.2—the virtual channel which has major number channel 4 and minor channel number 2—a user enters "4" with a number key 105, ":" with delimiter key 110, and then "2" with a number key 105.

FIG. 3 shows a process 300 for selecting a channel using channel commands, such as using channel command keys 120 as shown in FIG. 1A. When channel control circuit 165 receives a channel command, channel control circuit 165

determines the type of command (305). Channel control circuit 165 recognizes a predetermined set of commands, such as those which are available through remote control 100. Channel control circuit 165 processes the channel command to derive the desired channel (310). Channel control circuit passes the resulting channel number to channel processing circuit 170 as a channel number sequence (315).

An analog channel is sequentially before virtual channels with the same major channel number as the channel number of the analog channel. For example, when channel control circuit 165 has received a "+" command and the currently displayed channel is 4, channel control circuit 165 sends a request to channel processing circuit 170 for the next sequential channel. Channel processing circuit 170 checks whether virtual channel 4.1 is available and, if not, whether analog channel 5 is available, and so on. Channel processing circuit 170 returns the resulting channel number to channel control circuit 165, or alternatively can process the channel number directly.

FIG. 4 is a flowchart of a process 400 for selecting a virtual channel through a menu shown on a display, such as display 155 shown in FIG. 1B. When channel processing circuit 170 receives a physical channel number sequence from channel control circuit 165 (405), channel processing circuit 170 checks in the channel look up table 175 whether the selected physical channel is a digital or analog channel (410). If the physical channel is an analog channel, channel processing circuit 170 causes the tuner 160 to tune to the physical channel to display the broadcast signal on display 150 (415).

If the physical channel is a digital channel, channel processing circuit 170 causes display 150 to display a menu listing one or more virtual channels associated with that physical channel (420). To generate the menu, channel processing circuit 170 accesses the VCT of the transport stream on the physical channel. Alternatively, channel processing circuit 170 generates a full channel list of all the channels, virtual and analog, that have the same major channel number as the major channel number which corresponds to the selected physical channel.

In one implementation, channel processing circuit 170 always generates a full channel list for the selected physical channel, whether the physical channel is analog or digital. For example, in the case of an analog physical channel, channel processing circuit 170 obtains the major channel number corresponding to the selected analog physical channel from the channel look up table 175. Channel processing circuit 170 forms the full channel list by searching channel look up table 175 for all the virtual channels which have that major channel number.

Channel processing circuit 170 receives a selection from the menu made by the user (425). The user can select entries from menus in various ways, such as by using channel command keys 120 shown in FIG. 1A. Channel processing circuit 170 uses channel look up table 175 to find major and minor channel numbers corresponding to the selected entry and uses these numbers as a major and minor channel number sequence (430).

FIG. 5 is a flowchart of a process 500 for processing major and minor channel number sequences in a digital television, such as digital television 150 shown in FIG. 1B. After receiving a major and minor channel number sequence (502), channel processing circuit 170 identifies a physical channel and VCT associated with that sequence using channel lookup table 175 (505). For example, upon receiving the

major and minor channel number sequence "4.2" (i.e., a sequence having major and minor channel numbers 4 and 2, respectively), channel processing circuit 170 accesses channel lookup table 175 to determine the associated physical channel, such as physical channel 39. Channel processing circuit 170 also accesses the VCT for physical channel 39, such as through a pointer to the VCT stored in channel lookup table 175. Channel processing circuit 170 retrieves one or more packet identifiers ("PIDs") from the accessed VCT for packets in the transport stream on the selected physical channel which correspond to the selected virtual channel (510). As described above, a major and minor channel number sequence indicates a virtual channel. A single virtual channel can have associated multiple information streams. For example, the VCT may indicate that video data for the selected virtual channel has one PID and audio data has another PID.

Channel processing circuit 170 causes tuner 160 to tune to the selected physical channel (515). Channel processing circuit 170 extracts and decodes appropriate information from the signal received on the tuned physical channel using the retrieved PID or PIDs (520). Channel processing circuit 170 supplies this information to display 155 (525). Channel processing circuit 170 can also supply audio or other information to appropriate components of digital television 150.

The invention can be implemented in, or in combinations of, digital electronic circuitry, computer hardware, firmware, or software. An implementation can include one or more stored computer programs executable by a programmable system including a programmable processor and memory.

In the implementations described above, information describing virtual channels and mapping between channel numbers and virtual channels and physical channels is carried in the PSIP of digital channels. In alternative implementations, however, this information can be supplied in various ways or in a combination of ways. This mapping information can be provided by out-of-band ("OOB") signaling, such as in CATV. Alternatively, the mapping information can be provided by in-band signals, such as program guide and mapping information provided on a portion of an analog or digital channel. The information can be provided in real time or periodically, on a single channel or multiple channels. For example, in one such implementation, the channel processing circuit of a digital television builds the channel look up table by combining the mapping information received on multiple channels. A person of ordinary skill in the art will know how to modify the components of the digital television described above to accommodate one or more of these alternative information sources, such as by including additional tuners or software to access and store the mapping information.

In another alternative implementation, the channel selection is used to select a channel without tuning to that channel. For example, a user can select a channel as described above for recording at some future time. In this case, the digital television does not necessarily tune to the selected channel at the time of selection.

This disclosure describes numerous implementations of the invention. However, these implementations are illustrative and not limiting. Additional variations are possible and will be apparent to one of ordinary skill in the appropriate art.

What is claimed is:

1. A digital television, comprising:

a display;

a tuner including a connection for an externally supplied broadcast signal, where the tuner provides a signal carried on a physical channel selected from the broadcast signal;

a channel control circuit which derives major and minor channel number sequences from received control signals, where a major and minor channel number sequence indicates a specific channel carried in the broadcast signal;

a channel processing circuit connected to the channel control circuit, the display, and the tuner, where the channel processing circuit determines, when a physical channel indicated at least

by the major channel number is digital, a major and minor channel number sequence by displaying a list of channels associated with the physical channel; receives a selection of a minor channel from the list,

and generates a major and minor channel number sequence based thereon.

2. The digital television of claim 1, where the received control signals include a major channel number, a delimiter, and a minor channel number.

3. The digital television of claim 1, where the received control signals include a major channel number and a menu selection which indicates a minor channel number.

4. The digital television of claim 1, where the channel processing circuit comprises a channel look up table which indicates correspondences between major and minor channel number sequences and physical channels.

5. The digital television of claim 4, where the channel look up table further indicates correspondences between major and minor channel number sequences and channels encoded in digital signals carried in the broadcast signal.

6. The digital television of claim 4, further comprising an integrated keypad for inputting the received control signals.

7. The digital television of claim 4, further comprising an input device which includes a keypad for inputting the received control signals.

8. A method for selecting a channel in a digital television, comprising:

inputting a major channel number which indicates a first physical channel carried on a broadcast signal; determining whether the physical channel is digital; if the physical channel is digital, presenting a list at least of minor channel numbers associated at least with the physical channel;

using the list, inputting a minor channel number such that a major and minor channel number sequence can be generated therefrom.

9. The method of claim 1, where the second physical channel is the same as the first physical channel.

10. The method of claim 1, further comprising inputting a completion command to complete selecting a channel.

11. The method of claim 1, further comprising transmitting the major channel number, the delimiter, and the minor channel number to a digital television.

12. The method of claim 11, where the major channel number, the delimiter, and the minor channel number are transmitted to the digital television together.

13. The method of claim 1, where the digital signal is a transport stream.

14. The method of claim 13, where a correspondence between the minor channel number and the channel is provided by a virtual channel table carried in the transport stream.

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15. A method for selecting a channel in a digital television, comprising:
receiving a physical channel number sequence which indicates a physical channel which has a corresponding major channel number;
identifying the physical channel as analog or digital; when the physical channel is digital, determining a major and minor channel number sequence by
displaying a menu listing one or more channels associated with the physical channel,
receiving a selection from the menu, where the selection corresponds to a channel which has a corresponding minor channel number, and
generating a major and minor channel number sequence from the major channel number corresponding to the physical channel and the minor channel number corresponding to the selection.

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16. The method of claim 15, further comprising tuning to the physical channel corresponding to the major and minor channel number sequence.

17. The method of claim 15, further comprising, when the physical channel is analog, causing a tuner to tune to the physical channel to supply a signal carried on the physical channel to a display.

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18. A system for selecting a channel in a digital television, comprising:
means for receiving a physical channel number sequence which indicates a physical channel which has a corresponding major channel number;
means for identifying the physical channel as analog or digital;
means for causing a tuner to tune to the physical channel to supply a signal carried on the physical channel to a display when the physical channel is analog;
means for determining a major and minor channel number sequence when the physical channel is digital, by displaying a menu listing one or more channels associated with the physical channel,
receiving a selection from the menu, where the selection corresponds to a channel which has a corresponding minor channel number, and
generating a major and minor channel number sequence from the major channel number corresponding to the physical channel and the minor channel number corresponding to the selection.

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